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A Study of RF/Microwave Components Using Fused Deposition Modeling and Micro-Dispensing

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A Study of RF/Microwave Components Using
Fused Deposition Modeling and Micro-Dispensing

by

Joshua A. Stephenson

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering
Department of Electrical Engineering
College of Engineering
University of South Florida

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ABSTRACT

The design and study of multiple RF direct digital manufactured (DDM) devices are presented in this work. A 2.45 GHz, 180° hybrid coupler is designed to provide the space required for other system components. The coupler is designed and manufactured on a 32 mil Rogers 4003C substrate and adapted to a 100% in-fill acrylonitrile butadiene styrene (ABS) substrate. A size reduction of 66% is accomplished with a bandwidth of 16%. A DDM Ku band connector is modeled and fabricated using varying relative dielectric constants of 50% and 100% in-fill ABS. The connector maintains less than 0.45 dB of insertion loss up to 14 GHz and greater than 10dB of return loss up to 15 GHz. A lumped component model is also developed to model the damaged transition of the connector with agreement to numerical electromagnetic simulation software. Lastly, a thermal and RF study of a Ku band power amplifier (PA) is performed. Two 5 mil 100% in-fill ABS PA test fixtures are fabricated with a varying number of vias. The designs are biased at various operating points to collect thermal and RF data. The PA operates at 151°C before melting the ABS substrate. A thermal model is developed from the measurement data to predict the temperatures at given power levels with good agreement between simulation and model data.

CHAPTER 1: INTRODUCTION

3D printing is a well-known term from hobbyists to scientists and engineers. However, not so common knowledge is that 3D printing and rapid prototyping (RP) have been around since the late 1980's. The first RP technology was the stereolithography (SL) machine first patented by Charles Hull in 1984. The SL machine uses a UV curable liquid and a focused UV light to create 3D objects layer by layer [1]. In 1989, the famous fused deposition modeling (FDM) technology was invented by Scott Crump [2]. Since then, the patent has expired and many industries have moved in to take advantage of the technology. From aerospace to biological devices, 3D printing is applicable in many fields. 3D printing isn't a replacement for traditional high yield manufacturing processes. However, there is a clear benefit of 3D printing when manufacturing low volume highly customized parts or for rapid prototyping of a concept design to later build with traditional manufacturing methods.

1.1 Thesis Overview and Contributions

The purpose of this thesis is the use of direct digital manufacturing (DDM) to design RF and microwave devices. 3D printing RF devices presents many challenges due to the stringent requirements on line dimensions, relative dielectric constants, conductivity and thermal properties. When operating at higher frequencies parts reduce in size and this increases manufacturing difficulty. To limit these challenges, a high precision printer is needed. The nScript 3Dn series printer with nFD and SmartPump Technologies enables the high precision extrusion

and dispensing of thermoplastics and conductive pastes, respectively [3, 4]. The thermoplastic used in this work is acrylonitrile butadiene styrene (ABS). Also used are DuPont CB028 silver conductor [5] which is micro-dispensed using the SmartPump and Epoxy Technology H20E epoxy [6] is used for assembly purposes. Chapter 2 will discuss the basic background of 3D printing and the technologies used.

When considering a design, the cost per area is a main contributor to design decisions. Additionally, when space isn't available it's important that designers find ways of miniaturizing components to meet design specifications and packaging requirements. The size reduction of a 2.45 GHz, 180° hybrid coupler is the first major contribution of this thesis, as presented in Chapter 3. The miniaturization of the hybrid coupler is accomplished by using capacitively loaded transmission lines. This reduces the size of the transmission lines while maintaining the phase characteristics.

The second major contribution of this thesis is the demonstration of a Ku band DDM connector. Chapter 4 examines the utility of the time domain reflectometry (TDR) tool in designing the connector. Multiple parameter sweeps are performed to provide insight into the contributing factors of impedance mismatches at discontinuities. Also, an embedded semicircular transition is developed to convert the impedances and electromagnetic field configurations of a coaxial connector to a microstrip line.

Chapter 5 details the last contribution of this thesis, with the study of the thermal performance of a Ku-band power amplifier (PA) and its effect on RF performance. A simulation model for the test fixture is also developed that can be used to determine if a given material will sufficiently diffuse the heat away from the PA chip.

Chapter 6 will conclude the thesis with a summary of the research and recommendations for future work. Appendix A provides information about assembly techniques used as well as special considerations when using simulation software. Appendix B provides information about the printing procedure for the DDM connector.

CHAPTER 2: DIRECT DIGITAL MANUFACTURING BACKGROUND

2.1 Introduction

There are multiple forms of direct digital manufacturing (DDM) with stereolithography (SL), selective laser sintering (SLM), and fused deposition modeling (FDM) being a few of the popular technologies [7]. All three technologies fabricate parts from CAD files layer-by-layer, however the process with which they build the 3D parts varies. SL uses a laser and photosensitive resin to build its parts. SL and SLM are alike, but instead of a photosensitive resin SLM uses a powdered material. FDM, the technology used in this work, uses a thermoplastic filament which is melted with an extrusion head. FDM typically builds the model from the bottom, however depending on the structure this can vary. Section 2.2 will introduce the FDM process and the required components. Section 2.3 will cover micro-dispensing of conductive pastes that are used mainly for transmission lines and to fill via holes.

2.2 Fused Deposition Modeling

FDM is an extrusion based 3D printing technology. Figure 2.1 shows a basic desktop 3D printer setup. There are many different thermoplastic filaments available to include: acrylonitrile butadiene styrene (ABS), polylactic acid (PLA) and polyetherimide (ULTEM). Filaments are sold by the spool and are fed into the filament feeding system. The filament feeding system consists of various components to pull the filament from the spool to the heating element. Depending on

the type of material used, the heating element temperature will be adjusted to maintain flow of the material onto the heated print bed. From there the model will be built from the bottom up.

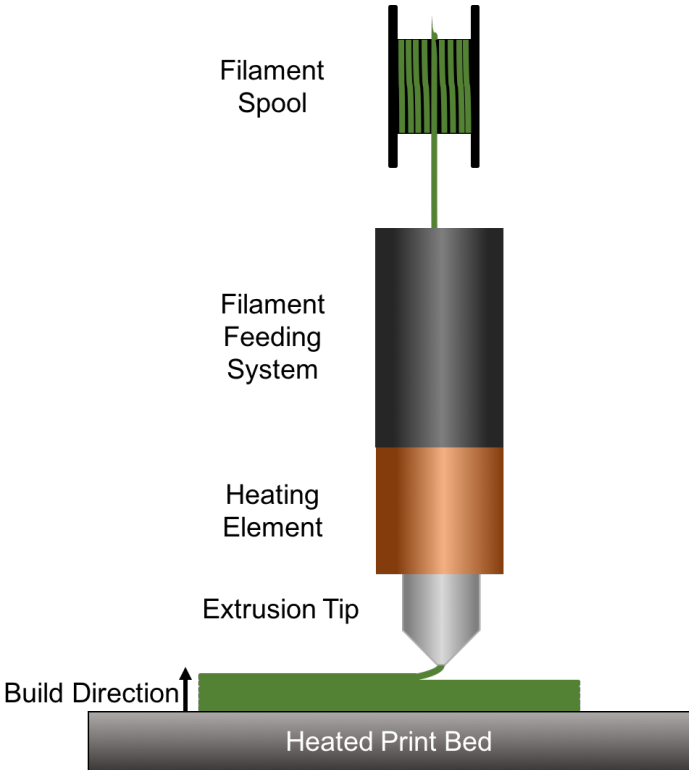


Figure 2.1 Basic desktop 3D printer setup

3D printing technology provides a designer with many options to customize designs. One such customization is in-fill percentage. In-fill percentage is the amount of material which will be used to fill the inside of the model. Figure 2.2a shows three different in-fill percentages of a rectilinear fill pattern. The fill pattern is exactly what it sounds like, the pattern that will be used to fill the inside of the model. Figure 2.2b shows the three fill patterns which are just a few of many types. The fill pattern will maintain the in-fill percentage regardless of the pattern chosen. By varying the in-fill percentage, the dielectric constant can be changed to accommodate the design. Both 50% and 100% in-fill percentages are used in this work, with a rectilinear pattern (Figure 2.2a).

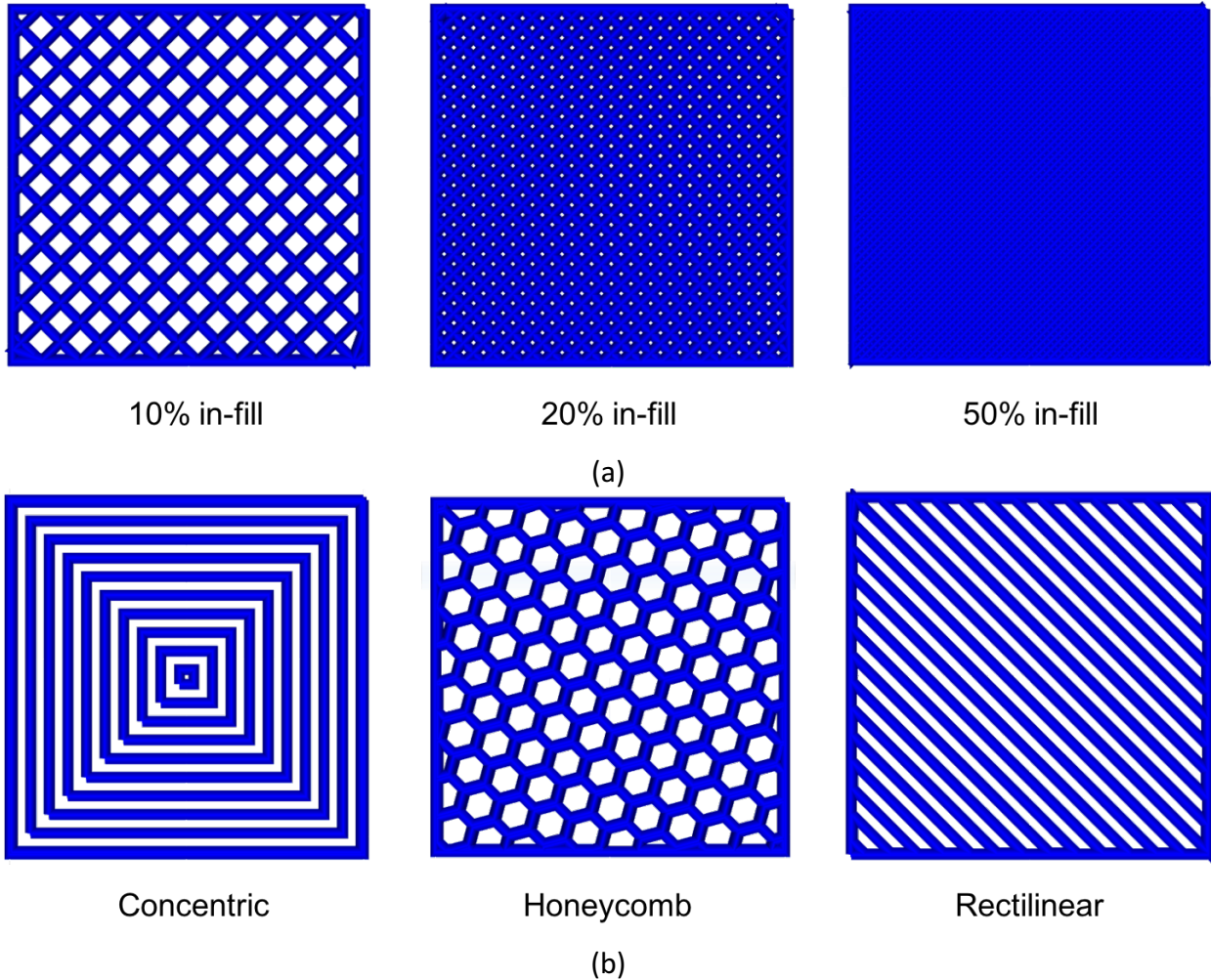


Figure 2.2 3D printer design settings. (a) varying in-fill percentage (b) varying in-fill pattern

The 3D printing system used in the presented research is the nScript 3Dn series. The nScript system utilizes a filament feeding system called the nFD. The nFD movement is restricted to the z-axis only. Where the heated print bed restricts movement to the x-y axis. The x-y resolution of the nScript printer is $10 \text{ nm} - 1 \text{ }\mu\text{m}$ and in the z direction is $0.5 \text{ }\mu\text{m}$ [8]. This high resolution provides the precision needed to print quality RF and microwave devices.

2.3 Micro-Dispensing

Micro-dispensing is a technology that enables the user to print a variety of materials with varying viscosities including epoxies and conductive inks with high precision. The ability to print

lines as small as 25 μm is possible with nScript SmartPump technology [4]. The configuration of the micro-dispensing system is shown in Figure 2.3. Conductive ink, e.g. DuPont CB028, is loaded into a syringe and connected to the SmartPump. A computer controls the dispensing according to an input file of the electronic circuit the user would like to print.

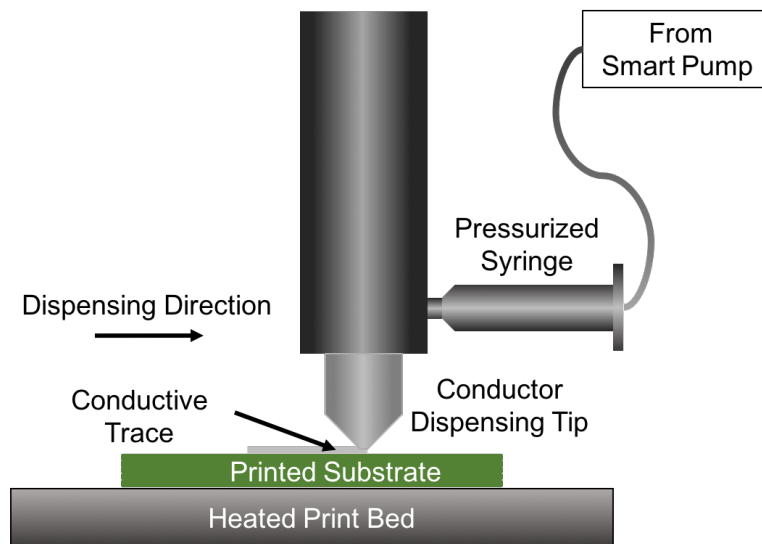


Figure 2.3 Micro-dispensing system used to print conductive ink

2.4 Conclusion

FDM and micro-dispensing alone are powerful technologies, but together the possibilities are endless. 3D printing provides the designer with added flexibility in the types of structures that are possible. Varying the in-fill percentage allows the dielectric constant to be varied layer-by-layer. Multiple layers of thermoplastics and conductive inks provide flexibility and a low-cost solution to traditional manufacturing technologies. Lastly, it provides the ability to print multi-material circuits and decreases the time to a first pass design.

CHAPTER 3: 2.45 GHZ HYBRID COUPLER

3.1 Introduction

Couplers are not new to microwave engineering. They have been used in various designs throughout history to include: baluns, mixers, and amplifiers [9, 10]. The topologies of hybrids provide either 0° , 90° or 180° phase difference at the output ports. The focus of this research is in a DDM fabricated 180° hybrid coupler that is used to feed the two ports of a circularly polarized antenna. The coupler operating frequency is 2.45 GHz and requires a $180 \pm 5^\circ$ phase difference between the coupled and through ports. The main driving requirement of the design is the size of the coupler, which needs to be less than 736 mm^2 . The small size will provide the space needed for other system components on a phased array unit cell. In section 3.2 the general theory behind the hybrid coupler will be presented. A brief derivation will be discussed to provide a basis for its operation. A variety of techniques to reduce the size of the coupler will be discussed in Section 3.3. Although the coupler will be fabricated using DDM, it is important to fabricate the coupler using traditional (subtractive) printed circuit board (PCB) manufacturing techniques for comparison. Section 3.4 is a discussion on the simulation and measurement results of the PCB version of the coupler. Section 3.5 provides the simulation versus measured results of the DDM coupler.

3.2 Hybrid Coupler Background

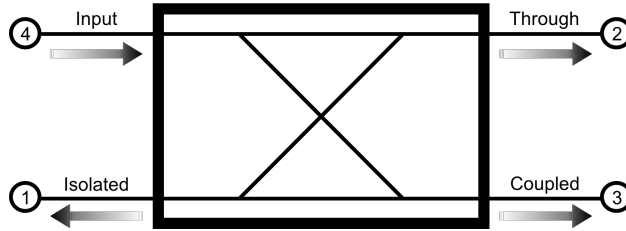


Figure 3.1 4-port network for a directional coupler

Directional couplers are 4-port devices (Figure 3.1) that can be reciprocal, matched at all ports and lossless under specific conditions. The derivation of the directional coupler, as discussed in [11], will be presented below. The S-parameter matrix of a 4-port network can be simplified if it's reciprocal ($S_{ij} = S_{ji}$):

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{22} & S_{23} & S_{24} \\ S_{13} & S_{23} & S_{33} & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix} \quad (3.1)$$

and matched at all ports, resulting in a diagonal matrix ($S_{ij}=0$ where $i = j$):

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & S_{23} & S_{24} \\ S_{13} & S_{23} & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & 0 \end{bmatrix} \quad (3.2)$$

If the network is lossless it needs to satisfy the unitary properties in equations 3.3 and 3.4.

$$\sum_{k=1}^N S_{ki} S_{kj}^* = 0, \text{ for } i \neq j \quad (3.3)$$

$$\sum_{k=1}^N S_{ki} S_{ki}^* = 1 \quad (3.4)$$

Applying equation 3.3 to the matrix in 3.2 results in equations 3.5-3.6 below:

$$S_{14}^* (|S_{13}|^2 - |S_{24}|^2) = 0 \quad (3.5)$$

$$S_{23} (|S_{12}|^2 - |S_{34}|^2) = 0 \quad (3.6)$$

One solution to 3.5 and 3.6 is that S_{14} and $S_{23} = 0$. This solution further simplifies the S-parameter matrix of 3.2, shown below:

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & 0 \\ S_{12} & 0 & 0 & S_{24} \\ S_{13} & 0 & 0 & S_{34} \\ 0 & S_{24} & S_{34} & 0 \end{bmatrix} \quad (3.7)$$

Applying equation 1.4 to the matrix in 1.7, results in equations 1.8-1.11:

$$|S_{12}|^2 + |S_{13}|^2 = 1 \quad (3.8)$$

$$|S_{12}|^2 + |S_{24}|^2 = 1 \quad (3.9)$$

$$|S_{13}|^2 + |S_{34}|^2 = 1 \quad (3.10)$$

$$|S_{24}|^2 + |S_{34}|^2 = 1 \quad (3.11)$$

The following relationships emerge when solving the system of equations: $|S_{13}| = |S_{24}|$ and $|S_{12}| = |S_{34}|$. After further simplification and selection of the phase constants, the following matrix results:

$$[S] = \begin{bmatrix} 0 & \alpha & \beta & 0 \\ \alpha & 0 & 0 & -\beta \\ \beta & 0 & 0 & \alpha \\ 0 & -\beta & \alpha & 0 \end{bmatrix} \quad (3.12)$$

where α and β are real constants. The above matrix is also known as an antisymmetric coupler due to the 180° phase difference between S_{13} and S_{24} . The above matrix is the basis for the hybrid coupler and will be used in the design process.

What the matrix in 3.12 describes is that depending on the input port(s) chosen, the designer can combine or divide the input power between a port(s) with a phase shift that depends on the phase reference of the output port(s). For example, if port 1 is chosen to be the input port, the power will be split between ports 2 and 3, and both output ports will be in phase.

However, if the input port is chosen to be port 4, the power will be split between ports 2 and 3, and the two signals will be 180° out of phase.

To determine how the power is divided the designer can change the coupling factor and utilize the conservation of power to determine the power split between ports, equations 3.13 and 3.14, respectively.

$$C = -20\log(\beta) \text{ dB} \quad (3.13)$$

$$|\alpha|^2 + |\beta|^2 = 1 \quad (3.14)$$

The coupling factor used for this application will be 3 dB. Utilizing the two equations above, $\alpha = \beta = 0.5$. Matrix 3.12 can then be simplified to:

$$[S] = \frac{j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix} \quad (3.15)$$

The matrix in 3.15 shows that when an excitation is applied to any one port, the resulting outputs will be half the power and either in phase or out of phase, depending on the input port.

3.3 Modified Directional Coupler

A popular topology for a 180° hybrid coupler is the ring hybrid or rat race (Figure 3.2). The ring hybrid has the behavior of the S-parameter matrix in 3.15. This section will cover the topology and simulation information for the 3 dB ring hybrid and the modified ring hybrid.

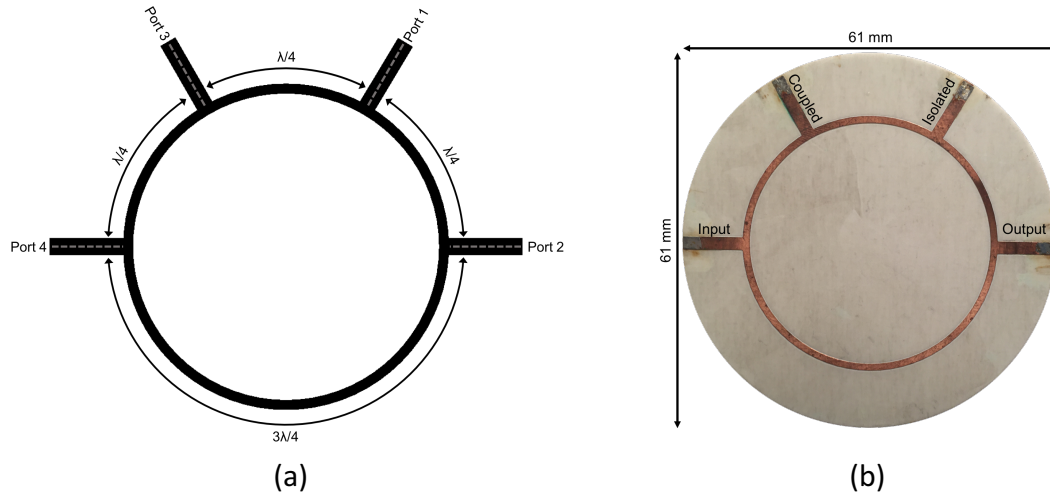


Figure 3.2 3 dB hybrid ring coupler. (a) layout (b) fabricated

Table 3.1 Design requirements for the 3 dB hybrid coupler

Parameter	Requirements
Layout Size	$< 736 \text{ mm}^2$
Coupling	$< 4 \text{ dB}$
Return Loss	$> 10 \text{ dB}$
Phase Difference ($^\circ$)	$180^\circ \pm 5^\circ$
Bandwidth	15%

The design requirements for the coupler are in Table 3.1. Keysight Advanced Design System (ADS) is used to realize the circuit in Figure 3.2. The substrate used for this simulation is the Rogers 4725JXR, whose material properties can be found in Table 3.2 [12]. ADS Linecalc is used to determine the widths and lengths of the various microstrip lines. The same dimensions and lengths can be calculated/verified using the various equations in [11]. The resulting microstrip dimensions are shown in Table 3.3.

Table 3.2 Material properties of the Rogers 4725JXR laminate

Parameter	Value
Dielectric Constant (E_r)	2.64
Substrate Height (H)	30.7 mil
Conductor Thickness (T)	25 μm
Conductivity (κ)	$5.8 \times 10^7 \text{ Sm}^{-1}$
Loss Tangent (TanD)	0.002

Table 3.3 Dimensions and characteristic impedance of the 3 dB ring hybrid

Microstrip Line	Z_0	Width	Arc Length
$\lambda/4$	70.71 Ω	1.11 mm	21.21 mm
$3\lambda/2$	70.71 Ω	1.11 mm	63.62 mm
Ports	50 Ω	2.09 mm	9.47 mm

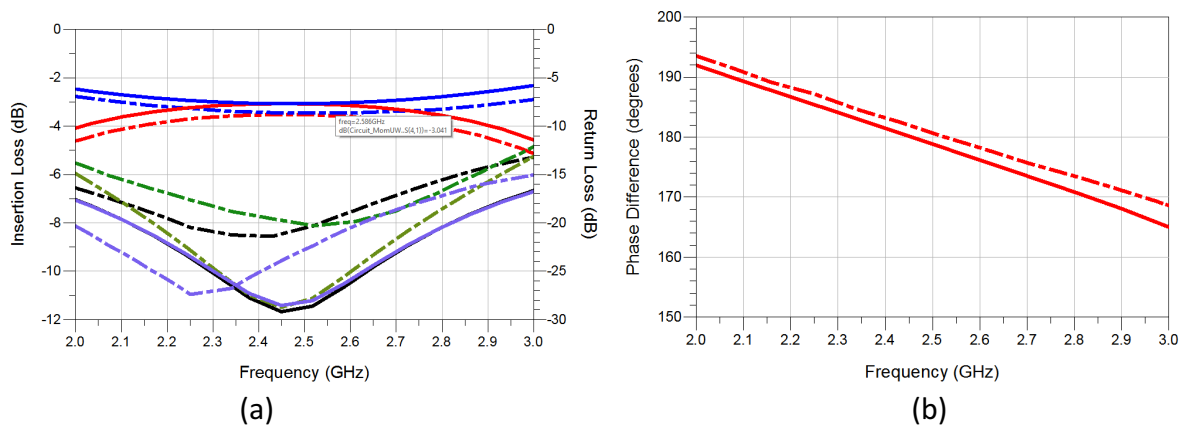


Figure 3.3 Simulated vs measured results of the 3 dB hybrid ring coupler.
 (a) S44, S24, S34 (b) Unwrapped phase difference between output ports
 Solid – Simulated Dashed – Measured

Table 3.4 Design requirements and achieved performance of the ring hybrid

Parameter	Requirements	Achieved
Layout Size	< 736 mm ²	3721 mm ²
Coupling	< 4 dB	< 4 dB
Return Loss	> 10 dB	> 15 dB
Phase Difference (°)	180° ± 5°	180° ± 5°
Bandwidth	15%	16%

The 3dB hybrid ring coupler is simulated using an ADS momentum simulation. The simulated vs measurement results for the circuit in Figure 3.2 are shown in Figure 3.3. The simulation shows that the power division between the two outputs is 3 dB. Whereas, the measurements have an output power of 3.5 dB at the center frequency (Figure 3.3a). Although, the overall trend of the power split shows agreement. Figure 3.3b shows the unwrapped phase difference between the two output ports. The phase difference of the simulated and measured circuit is 179.8° and 182° at the center frequency, respectively. Table 3.4 summarizes the results and design goals.

Although the rat race coupler provides sufficient performance the size of the coupler is too large. To meet this requirement, the circuit will need to be modified to reduce the size while maintaining the RF performance. This will be accomplished through miniaturization techniques such as capacitive loading [10]. By capacitive loading the transmission line (TL), the designer will, in effect, reduce the length while maintaining the same phase delay. Figure 3.4 shows the topology of a $\lambda/4$ transmission line and the associated ABCD matrix. The equivalent circuit and associated ABCD matrix used to miniaturize the $\lambda/4$ transmission line is shown in Figure 3.5.

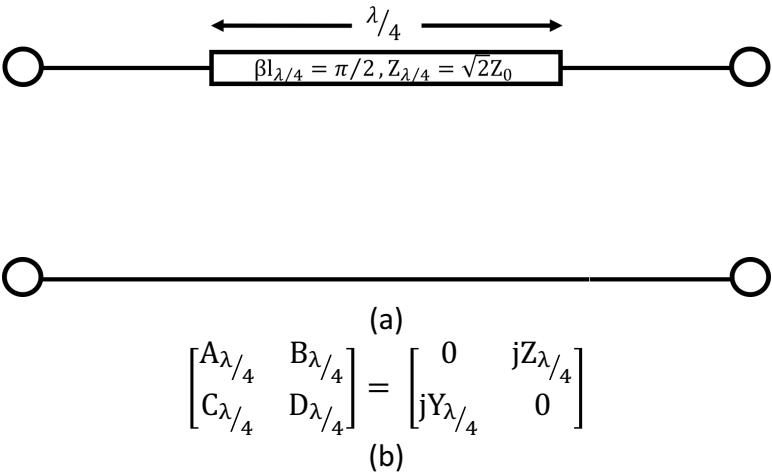
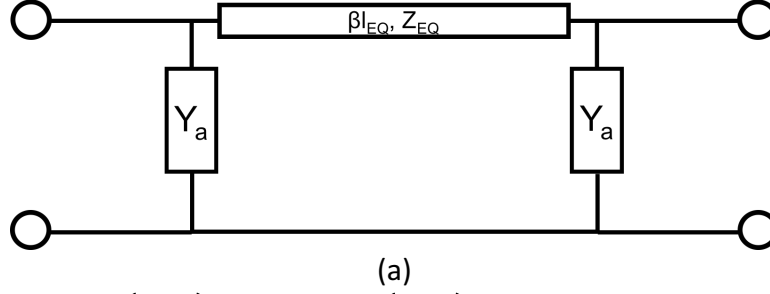


Figure 3.4 $\lambda/4$ transmission line used in the hybrid coupler.
 (a) equivalent circuit (b) ABCD matrix



$$\begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} = \begin{bmatrix} \cos(\beta l_{EQ}) + jY_a Z_{EQ} \sin(\beta l_{EQ}) & jZ_{EQ} \sin(\beta l_{EQ}) \\ 2Y_a \cos(\beta l_{EQ}) + j \sin(\beta l_{EQ}) (Y_{EQ} + Y_a^2 Z_{EQ}) & jY_a Z_{EQ} \sin(\beta l_{EQ}) + \cos(\beta l_{EQ}) \end{bmatrix} \quad (b)$$

Figure 3.5 $\lambda/4$ equivalent circuit. (a) network topology (b) ABCD matrix

For the two transmission lines to exhibit the same RF behavior the ABCD matrix of the two networks must be equal:

$$\cos(\beta l_{EQ}) + jZ_{EQ} Y_a \sin(\beta l_{EQ}) = 0 \quad (3.16)$$

$$jZ_{EQ} \sin(\beta l_{EQ}) = jZ_{\lambda/4} \quad (3.17)$$

$$2Y_a \cos(\beta l_{EQ}) + jY_{EQ} \sin(\beta l_{EQ}) + jY_a^2 Z_{EQ} \sin(\beta l_{EQ}) = jY_{\lambda/4} \quad (3.18)$$

$$jY_a Z_{EQ} \sin(\beta l_{EQ}) + \cos(\beta l_{EQ}) = 0 \quad (3.19)$$

Solving equations 3.16-3.19 for Z_{EQ} , Y_a , and l_{EQ} , results in the following relationships:

$$l_{EQ} = \frac{\lambda}{8} \quad (3.20)$$

$$Z_{EQ} = 2Z_0 \quad (3.21)$$

$$C_a = \frac{1}{2\omega_0 Z_0} \quad (3.22)$$

The solutions to the equivalent network in Figure 3.5 result in a transmission line which is half of the size of the previous rat race coupler TL. This is possible due to the shunt capacitances defined by Equation 3.22. A similar procedure is used for the $3\lambda/4$ TL of the ring hybrid in Figure 3.2. Figure 3.6 shows the $3\lambda/4$ TL and the respective ABCD matrix. The equivalent pi network that

can be implemented to minimize the physical length of the transmission line is shown in Figure 3.7, along with its ABCD matrix.

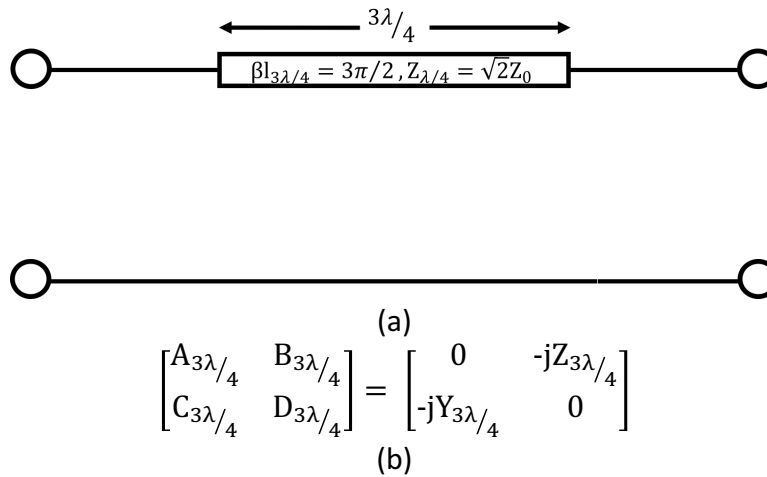


Figure 3.6 $3\lambda/4$ transmission line used in the hybrid coupler. (a) equivalent circuit (b) ABCD matrix

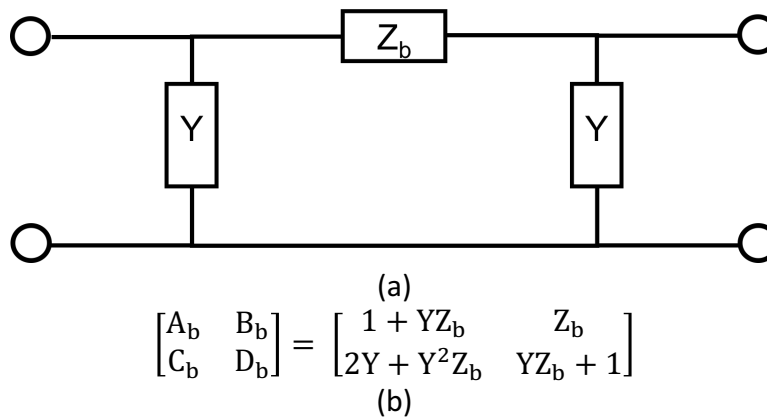


Figure 3.7 $3\lambda/4$ equivalent circuit. (a) network topology (b) ABCD matrix

After equating the two matrices (3.6b and 3.7b) and solving the resulting equations the following relations are obtained:

$$L = \frac{\sqrt{2}Z_0}{\omega_0} \quad (3.23)$$

$$C_b = \frac{1}{\sqrt{2}\omega_0 Z_0} \quad (3.24)$$

Using equations 3.20-3.24, and the equivalent networks for the $\lambda/4$ and $3\lambda/4$ the miniaturized ring hybrid is determined, as shown in Figure 3.8.

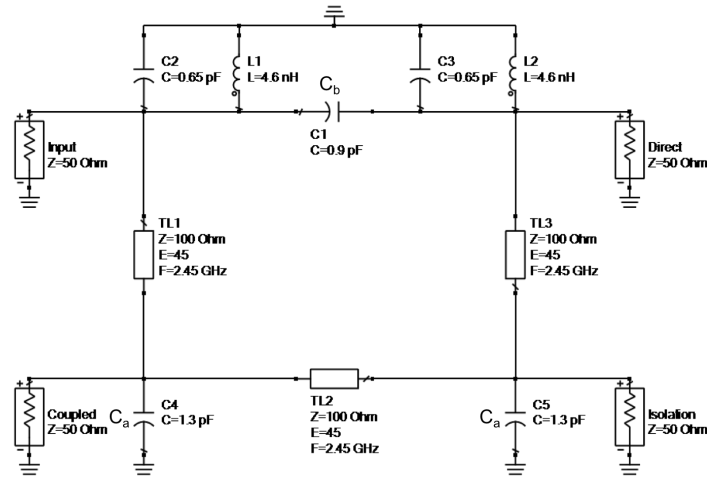


Figure 3.8 Miniaturized ring hybrid with parallel inductors and capacitors

The circuit topology of Figure 3.8 is simulated in an ADS schematic using ideal components (capacitors, inductors, TL). The coupler is simulated using ADS and the results are shown in Figure 3.9. The capacitances, inductances and transmission line properties/values are calculated using the equations derived above. Figure 3.9a shows that the power is equally split with the insertion losses being approximately 3 dB at the design frequency of 2.45 GHz. The phase difference between the output ports is within $\pm 5^\circ$ across the entire bandwidth (Figure 3.9b).

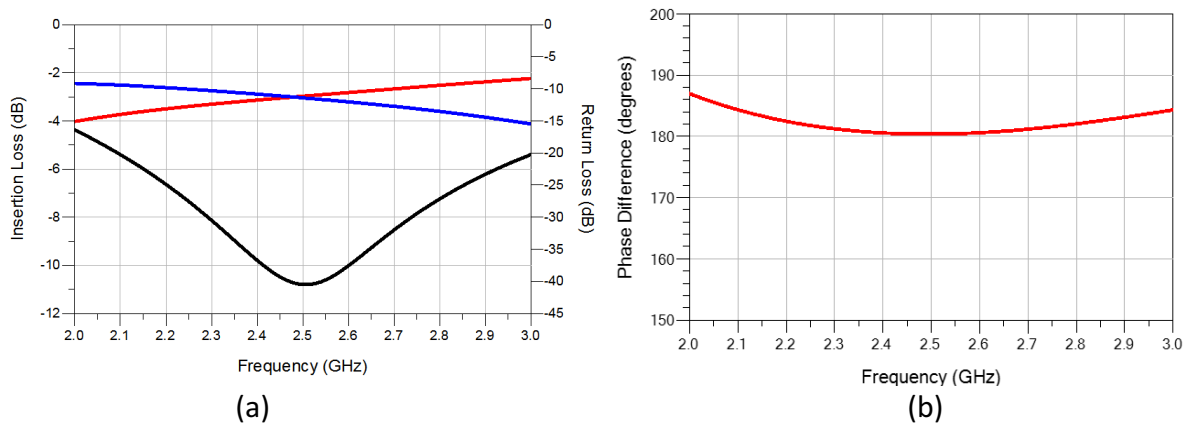


Figure 3.9 Simulated results of the ideal 3 dB modified hybrid. (a) Insertion and Return Loss (b) Unwrapped phase difference between output ports

The impedance of the of the parallel LC is high at the design frequency, allowing for the circuit in Figure 3.8 to be simplified, by removing the two components. The layout of the resulting circuit is shown in Figure 3.10.

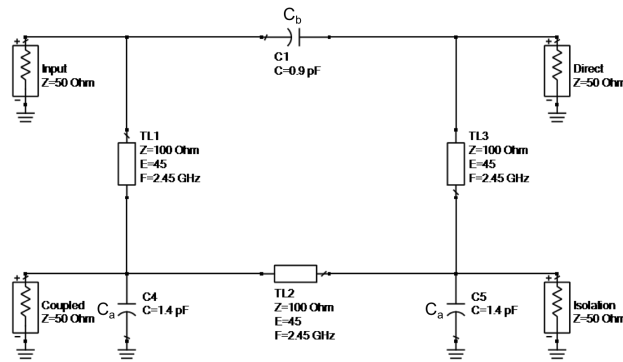


Figure 3.10 Miniaturized ring hybrid without parallel inductors and capacitors

The simulation results of the ADS schematic in Figure 3.10 are shown in Figure 3.11. Removing the parallel LC, changes the input return loss of the hybrid as well as the phase difference between the direct and coupled ports. The change in the phase difference can be compensated by changing the value of C_a to 1.5 pF and the lengths of the transmission lines to 47° (Figure 3.10). The simulation results of the modified hybrid are shown Figure 3.12. Removing the extra components will reduce the overall footprint of the overall coupler, however the phase performance degrades. This performance degradation can be addressed when parasitic components, interconnects and transmission line elements are introduced.

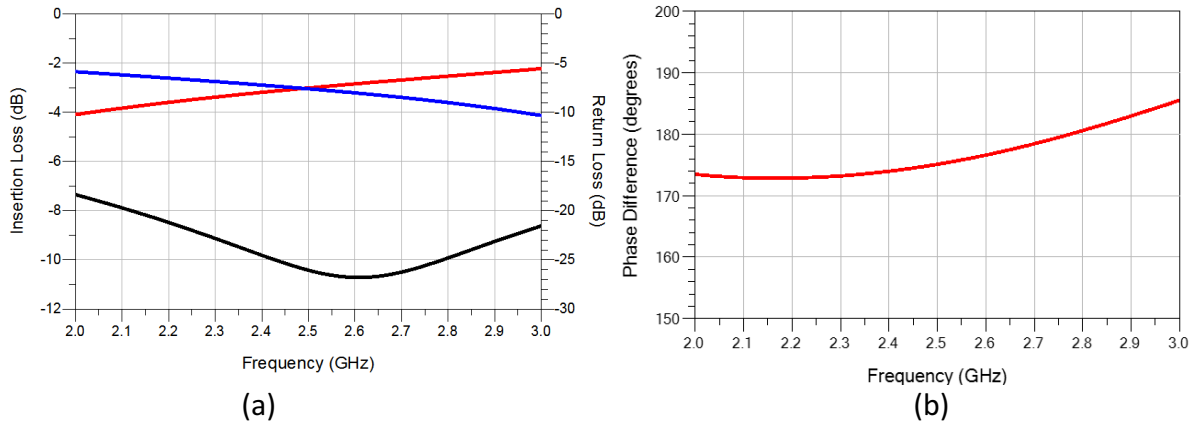


Figure 3.11 Simulation results of the ideal hybrid without parallel components.
 (a) Insertion and Return Loss (b) Unwrapped phase difference between output ports

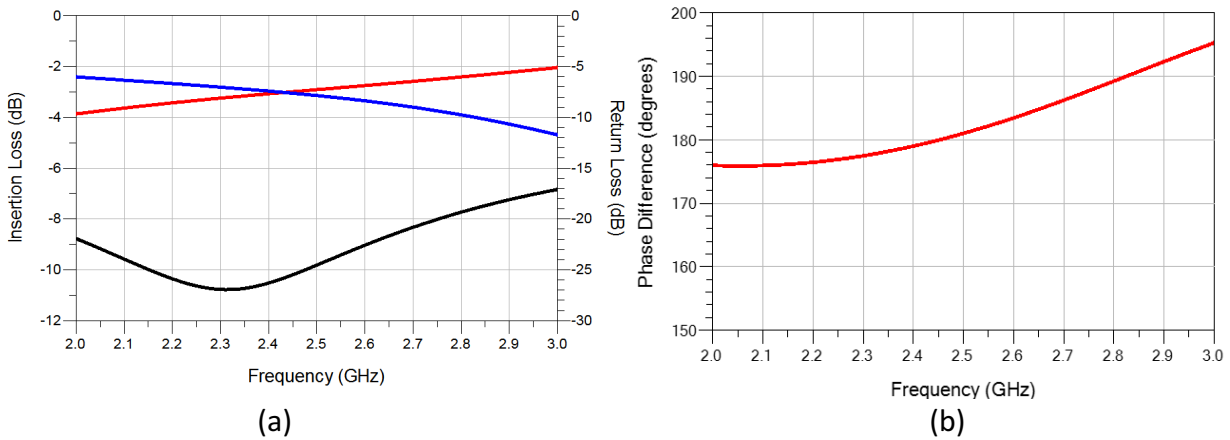


Figure 3.12 Simulation results of the modified ideal hybrid without parallel elements.
 (a) Insertion and Return Loss (b) Unwrapped phase difference between output ports

3.4 PCB Version Simulation and Measured Results

The previous sections provided the foundation for the design of a reduced size ring hybrid. In this section, the parasitic design, simulation, and measurement results are presented. The substrate used in the development of the design is a 32 mil Rogers 4003C laminate [13], whose substrate properties are summarized in Table 3.4. A $\lambda/8$ transmission line, at 2.45 GHz, has the following properties: length of 9.88 mm, width of 0.44 mm and an impedance of 100 Ω . The coupler in Figure 3.10 is physically unrealizable due to the transmission line elements. The straight transmission lines between the input and coupled ports, and direct and isolation ports

will not be connected in the form of Figure 3.10. This issue is solved using curved transmission line elements as shown in Figure 3.13. The tuned circuit schematic and layout are shown in Figure 3.13a and Figure 3.13b, respectively. When the exact dimensions and capacitor values are used from Figure 3.10 the performance of the circuits is degraded. The curved transmission line lengths and capacitor values need to be reduced with C_a , C_b and $L_{\lambda/4}$ changed to: 1 pF, 0.7 pF, and 9.48 mm, respectively. The simulated results of the tuned circuit are shown in Figure 3.14.

Table 3.5 Material properties of the Rogers 4003C laminate

Parameter	Value
Dielectric Constant (ϵ_r)	3.38
Substrate Height (H)	32 mil
Conductor Thickness (T)	35 μm
Conductivity (κ)	$5.8 \times 10^7 \text{ Sm}^{-1}$
Loss Tangent (TanD)	0.002

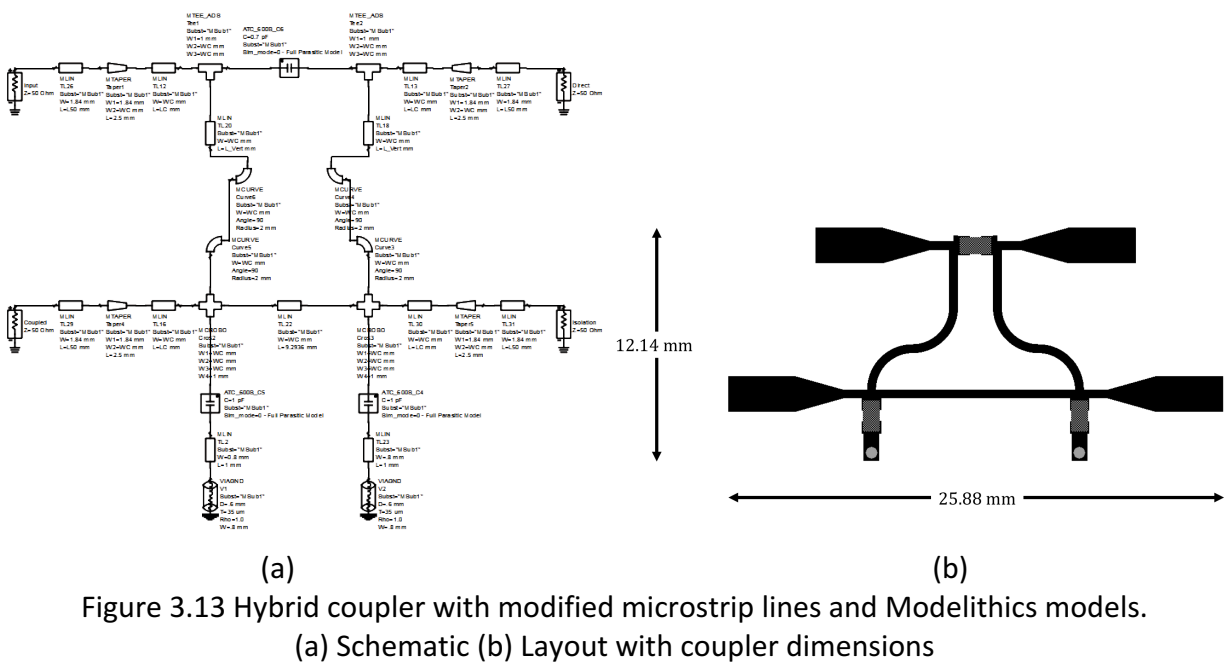


Figure 3.13 Hybrid coupler with modified microstrip lines and Modelithics models. (a) Schematic (b) Layout with coupler dimensions

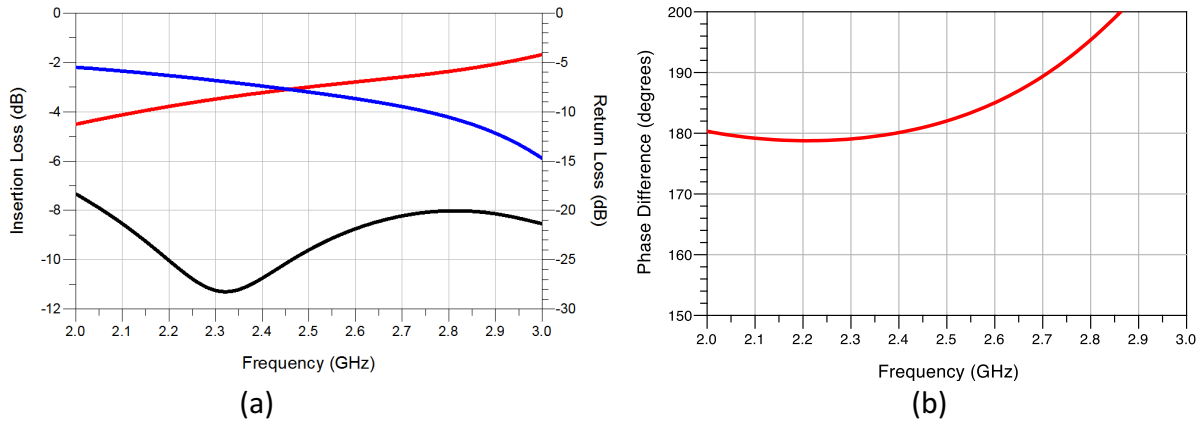


Figure 3.14 Simulation results of the modified hybrid with realistic elements.
 (a) Insertion and Return Loss (b) Unwrapped phase difference between output ports

The hybrid in Figure 3.13 has a coupling value, at 2.45 GHz, of 3.1 dB and a phase difference of 181° . The coupling value remains within 3 ± 1 dB across the bandwidth of the coupler.

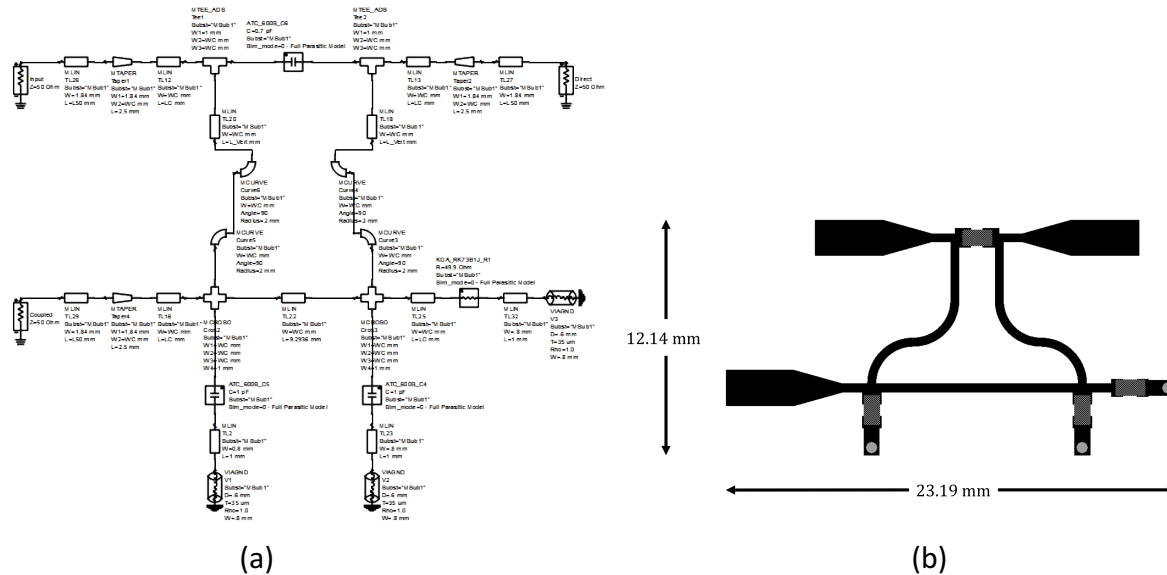


Figure 3.15 Hybrid coupler with the isolated port terminated in 49.9Ω .
 (a) Schematic (b) Layout with coupler dimensions

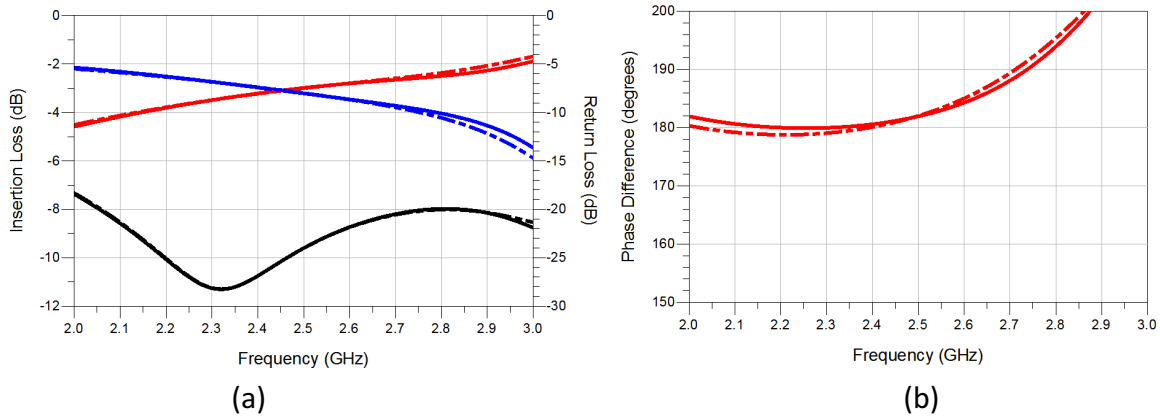


Figure 3.16 Comparison of the modified hybrid with and without a 49.9 Ω terminated isolation port. (a) Insertion and Return Loss (b) Unwrapped phase difference between output ports Solid – Without Termination Dashed – With Termination

The simulation data of the 4-port hybrid meets all the design requirements of Table 3.1. However, the coupler's application requires that the isolation port be terminated in 50 Ω, as shown in Figure 3.15. The simulation results in Figure 3.16 show that the changes in the coupling, return loss and phase difference between the 4-port hybrid and the terminated isolation port hybrid are minimal.

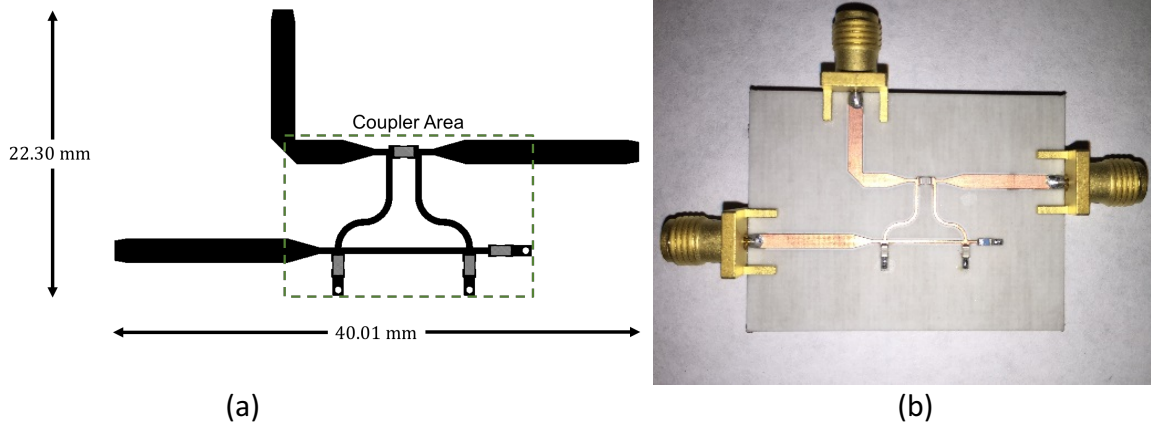


Figure 3.17 Layout and picture of the Rogers 4003C hybrid coupler. (a) Layout with dimensions of the PCB. (b) Picture of the fabricated hybrid coupler.

To fabricate the circuit, feedlines are added to the coupler. The layout and the fabricated coupler design are shown in Figures 3.17a and 3.17b, respectively. The ADS co-simulation and measured data are shown in Figure 3.18.

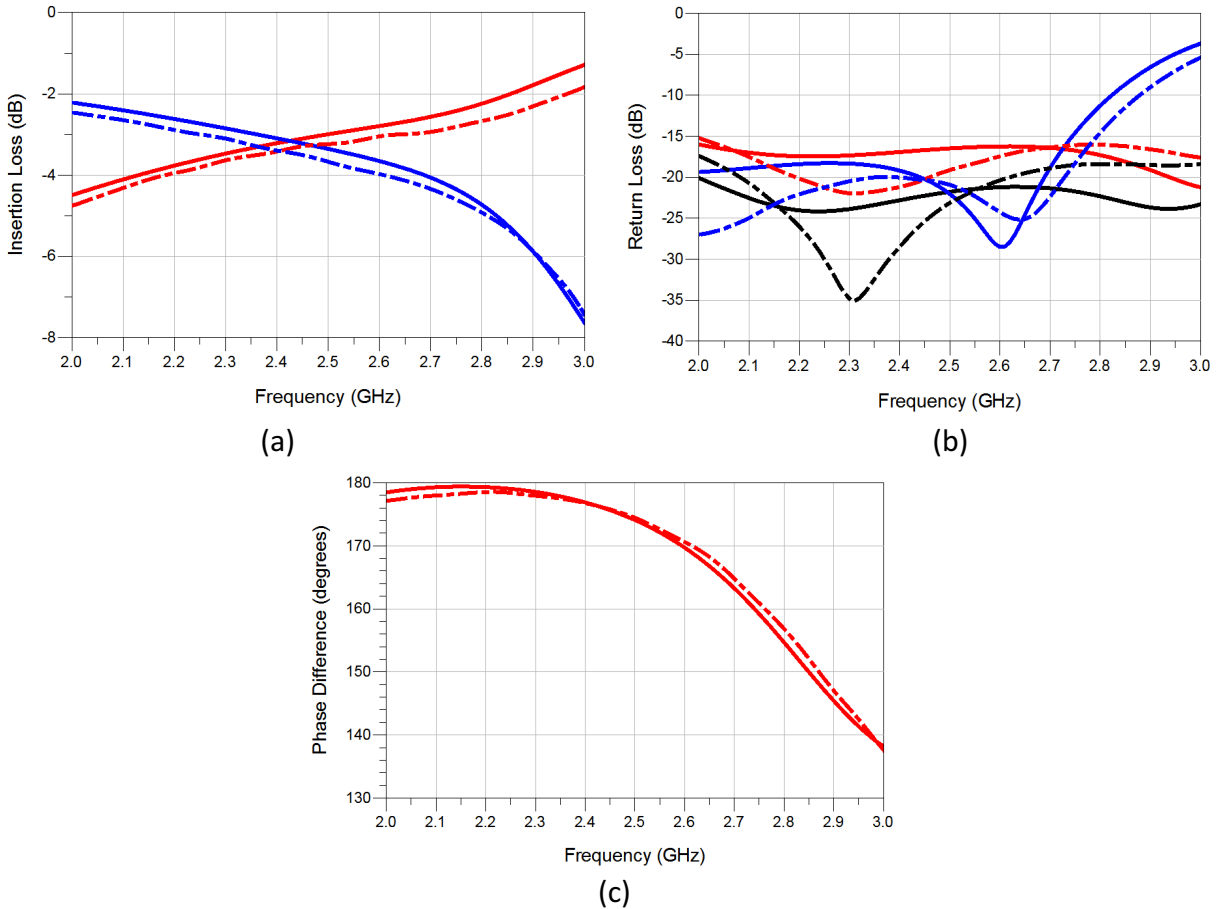


Figure 3.18 Simulated vs measurement data for the fabricated coupler.
 (a) Insertion Loss (b) Return Loss (c) Unwrapped phase difference between output ports
 Solid – Simulated Dashed – Measured

There is good agreement between the simulated and measured data. The crossover frequency for the insertion losses is approximately 30 MHz different (Figure 3.17a). However, the 3 dB split is maintained at the frequency of interest. The return loss of all ports is greater than 15 dB. The area of the Roger 4003C coupler is 231.35 mm^2 providing a substantial decrease compared to the rat race coupler of Section 3.3.

3.5 DDM Version Simulation vs Measurement Results

The DDM version of the coupler is much like the Rogers 4003C version. The main difference is in the width of the lines to maintain the 100 ohm impedance caused by the relative dielectric changes (Table 3.6).

Table 3.6 Material properties of 100% in-fill ABS

Parameter	Value
Dielectric Constant (ϵ_r)	2.423
Substrate Height (H)	32 mil
Conductor Thickness (T)	25 μm
Conductivity (κ)	$1.65 \times 10^6 \text{ Sm}^{-1}$
Loss Tangent (TanD)	0.006

The layout and the fabricated coupler design are shown in Figures 3.19a and 3.19b, respectively. The co-simulated and measured data are shown in Figure 3.20. The coupler area is 248.82 mm^2 which is 66% smaller than the requirement of 736 mm^2 . The capacitor values did not change between the PCB version and DDM version ($C_a = 1 \text{ pF}$ and $C_b = 0.7 \text{ pF}$).

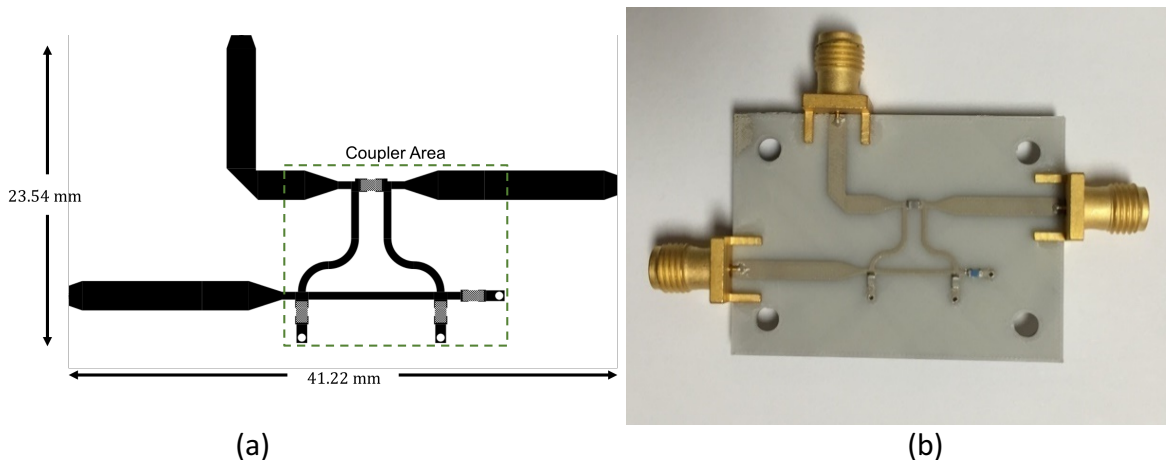


Figure 3.19 Layout and picture of the DDM hybrid coupler.

(a) Layout with dimensions of the DDM coupler. (b) Picture of the fabricated hybrid coupler.

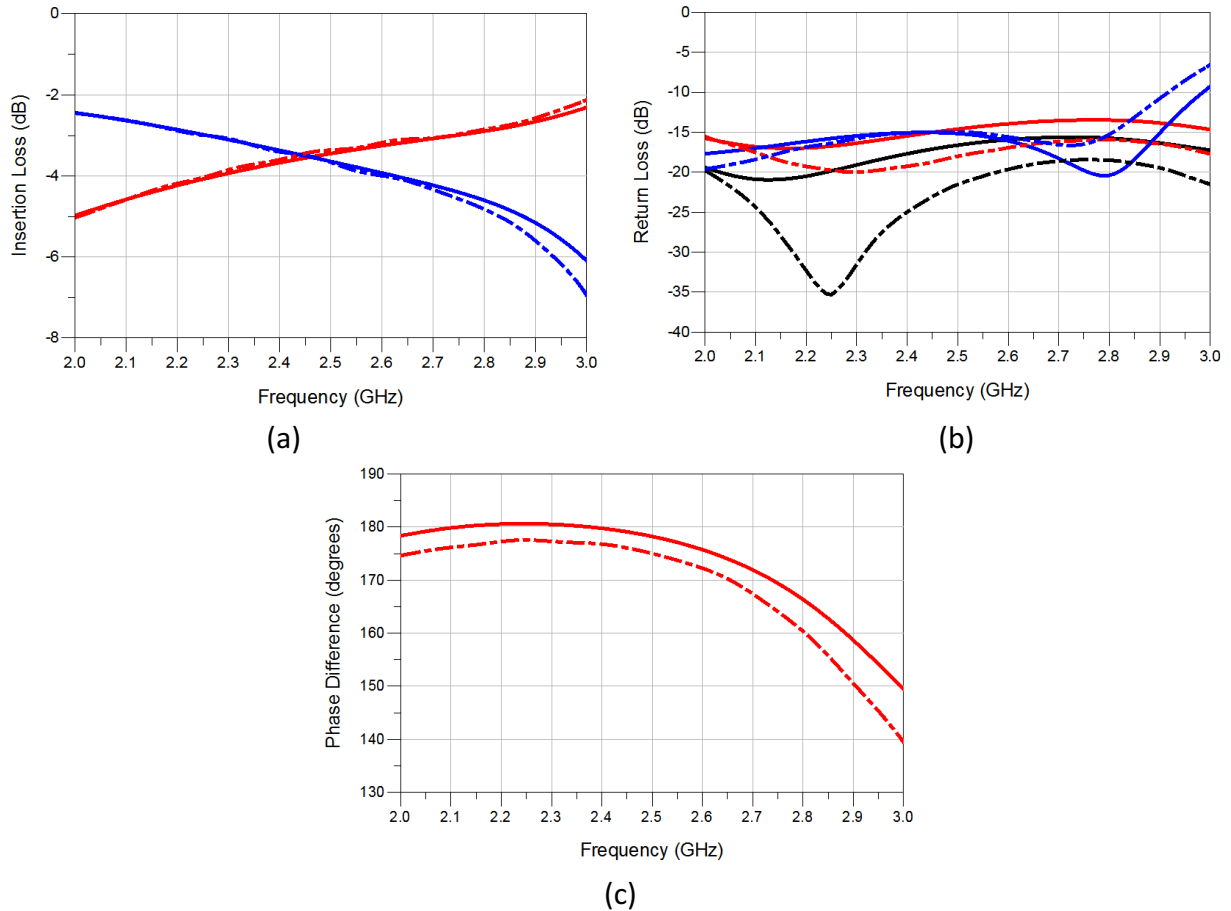


Figure 3.20 Simulated vs measurement data for the fabricated DDM coupler.
 (a) Insertion loss (b) Return loss (c) Unwrapped phase difference between output ports
 Solid – Simulated Dashed – Measured

The DDM coupler has good insertion and return losses at the design frequency and the measurement to simulated results share the same trend. The insertion loss bandwidth is approximately 16%. The return losses maintain 10 dB and greater up to 2.9 GHz. The measured phase difference of the coupler is below the 180°. In future designs, the transmission lines should be tuned to compensate for this low phase difference.

3.6 Conclusion

In this chapter, the design and fabrication of a 180° hybrid coupler was discussed. The general theory provided an understanding of the operation of the coupler. The rat race coupler provided a good starting point for further minimization techniques. Using lumped components and equivalent networks provided a means to reduce the size of the hybrid coupler while maintaining the performance of the coupler. Although, some of the components could be neglected to further reduce the size. This reduction in components and size comes at a cost of symmetry and performance. But, size is the driving requirement to the design so the performance degradation is acceptable. Both PCB and DDM versions of the reduced size coupler showed good simulation to measurement performance. However, in the future the output phase difference will need improvements.

CHAPTER 4: KU-BAND CONNECTOR

4.1 Introduction

Interest in 3D printing RF devices has grown over the past few years. The ability to 3D print filters, power dividers, antennas, and phase shifters has become common place [14-17]. However, a challenge that presents itself when testing or connecting these components to other modules, is a robust connector that can be embedded and printed with the design itself. For example, if each component on a unit cell needed to be tested, the designer would have to print the unit cell and buy off the shelf parts and assemble the connectors as a post processing step. However, if a 3D printed connector could be printed along with the structure all the user would have to do is connect the coaxial cable. This would reduce the time to testing and the unnecessary temperature exposure to cure the silver epoxies. In this chapter, the general design procedure of the DDM connector (Section 4.2), the design of the test structure (Section 4.3), the design considerations (Section 4.4), the simulated vs measured results (Section 4.5), and the transition modeling (Section 4.6) will be covered.

4.2 DDM Connector Design

The subminiature version a (SMA) to slip on adapter used for the design is the Konnect RF model number KAD178244, which has an upper frequency of 18 GHz [18]. The adapter is a SMA to slip-on adapter. The adapter is cross sectioned to determine the different dimensions that would be inaccessible otherwise. The adapter and a cross section of the adapter are shown in

Figure 4.1. The design of the Direct Digital Manufactured (DDM) connector is constrained by the dimensions of the commercial off-the-shelf (COTS) adapter (Figure 4.1a). The DDM connector will also be referred to as a receptacle in this work, however they refer to the same thing (Figure 4.2a). Table 4.1 lists the dimensions of a 50-ohm coaxial line as well as the DDM connector. The COTS adapter dimensions on the male end are used as the starting point for the DDM connector, which is designed using Computer Simulation Technology (CST) numerical electromagnetic simulation software. All TDR simulations are performed using CST and the S-parameter data is verified using Ansys High Frequency Structural Simulator (HFSS).

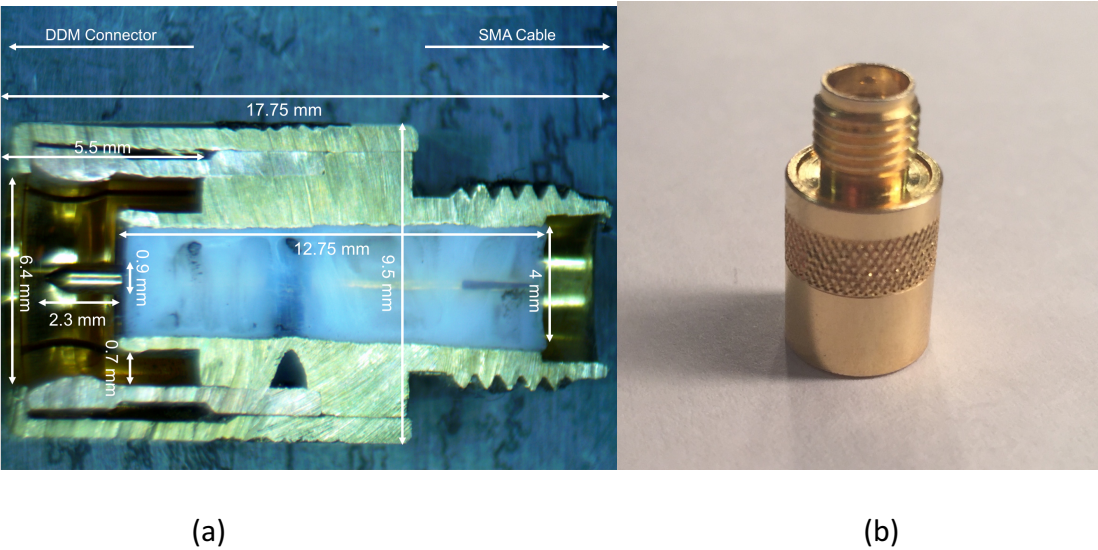


Figure 4.1 Konnect RF KAD178244 adapter used as an interface between an SMA assembly and the DDM connector. (a) cross-section (b) connector

Table 4.1 50-ohm coaxial line and DDM connector dimensions and parameters

Parameter	50-ohm coaxial line	DDM
Outer Diameter (mm)	4	6.2
Inner Diameter (mm)	1.25	1.7
Dielectric Constant	2.1	2.4
Loss Tangent	0.001	0.006
Length (mm)	12.75	4.5
Z_0 (ohm)	48.125	50.0

Understanding the limiting factors of the connector is accomplished by modeling the connector in CST and performing various simulations. To avoid an overly complicated model of the COTS adapter, a 50-ohm coaxial line is used in the simulations as outlined in Table 4.1. Similarly, the DDM receptacle is modeled using the tabulated data of Table 4.1.

The time domain reflectometry (TDR) plot of the connector provides insight into changes in impedance along the structure and the distance at which discontinuities occur. Equation 4.1 is used to understand the discontinuity and its effect on impedance [11]. If the impedance on a TDR plot results in a low impedance spike this is due to the capacitance increasing or the inductance decreasing in the transmission line. In contrast, if the impedance increases this is due to the inductance increasing or the capacitance decreasing.

$$Z = \sqrt{\frac{L}{C}} \quad (4.1)$$

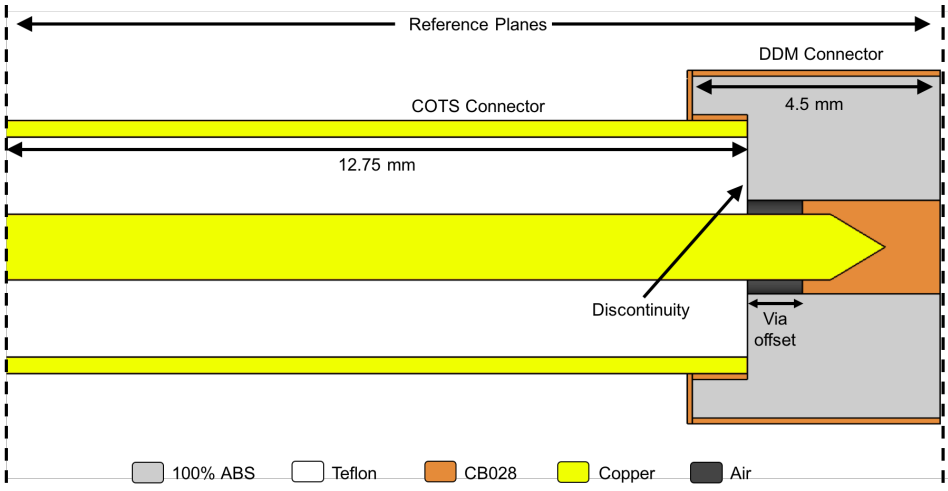
Equation 4.2 is used to determine the time to the discontinuity from the SMA end of the COTS adapter (Figure 4.1) [19]. The time calculated corresponds to the interface between the COTS adapter and DDM receptacle (Figure 4.2a). Where t is the time to the discontinuity, in seconds, l_n is the length of the n th material, in meters, and ϵ_r^n is the dielectric constant of the n th material. For example, from Table 4.1, the COTS adapter dielectric constant is 2.1 and has a length of 12.75 mm and the DDM connector dielectric constant is 2.4 and has a length of 4.5 mm. Using Equation 4.2, the time (t) to the discontinuity (Figure 4.2a) is 0.17ns.

$$t = \frac{2l_1\sqrt{\epsilon_r^1}}{c} + \frac{2l_2\sqrt{\epsilon_r^2}}{c} + \dots + \frac{2l_n\sqrt{\epsilon_r^n}}{c} \quad (4.2)$$

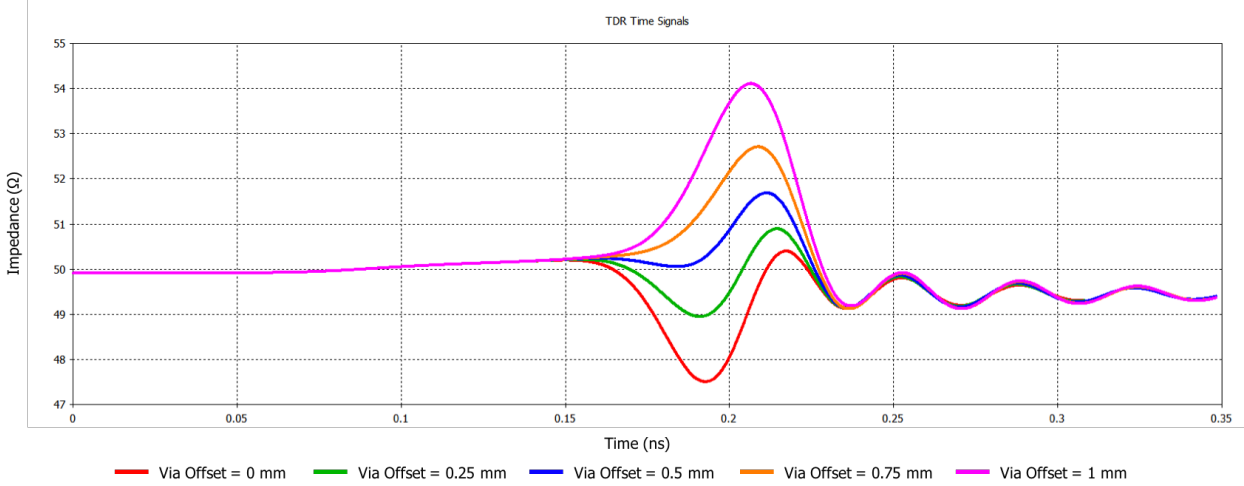
Figure 4.2, shows the model of the connector and the parametric sweep of the via offset.

As shown in Figure 4.2a, there is a discontinuity in both the size of the structures and the material

properties when connecting the COTS adapter to the DDM receptacle. The discontinuity causes a capacitance increase due to the higher relative dielectric constant of 100% in-fill ABS, resulting in an impedance reduction. Offsetting the via into the DDM connector results in extra inductance that counter acts the capacitive discontinuity. A smoother transition between the COTS adapter and the DDM receptacle results until the inductance becomes too large. Figure 4.2b shows that as the via inset is increased the impedance increases. The optimum value for the via offset is 0.25 mm.



(a)



(b)

Figure 4.2 Simulation model and results varying the via offset.
 (a) Initial DDM connector design (b) TDR plot of varying via offset

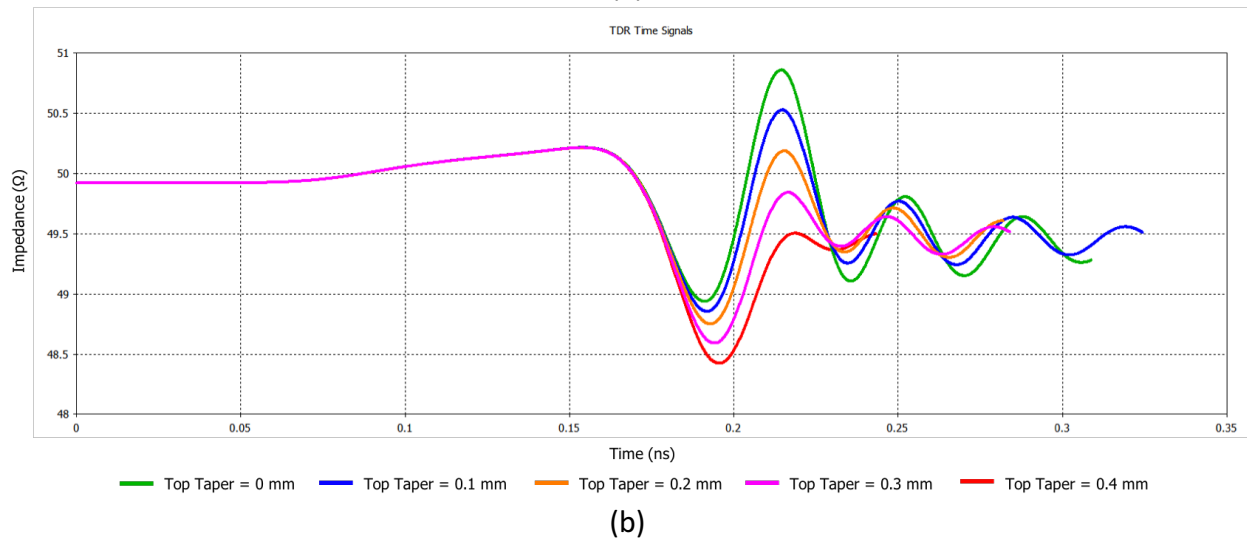
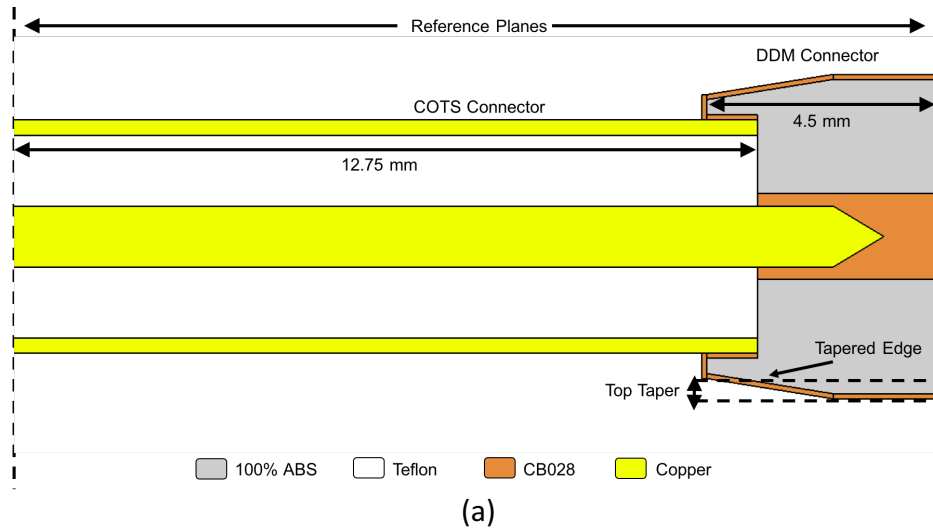


Figure 4.3 Simulation model and results varying the top taper.
 (a) Tapered DDM connector design (b) TDR Plot with varying the tapered edge

Tapering the DDM connector, as shown in Figure 4.3a, also minimizes the abrupt change in the impedance. Figure 4.3b shows the parametric sweep of the tapered edge. The top taper parameter is the difference between the outer radius of the DDM connector and the top radius of the taper (Figure 4.3a). Varying the taper doesn't significantly impact the impedance. However, the taper reduces the mechanical stresses introduced by the compression design of the slip-on connector. The COTS adapter in Figure 4.1a has a compression fitting on the DDM connector end. When mating the COTS adapter and the DDM connector the taper allows for a

smoother transition to the larger radius of the DDM connector. Without the taper, there would be a sharp edge at the COTS-DDM interface and there is a higher risk of damaging the top of the connector.

The analysis above shows that a via offset of 0.25 mm and a top taper of 0.4 mm are the optimum dimensions for the connector interface. The S-parameter performance of the COTS-DDM structure, with these modifications, is shown in Figure 4.4. The design results in a return loss of 23.8 dB and an insertion loss of 0.2 dB at 18 GHz.

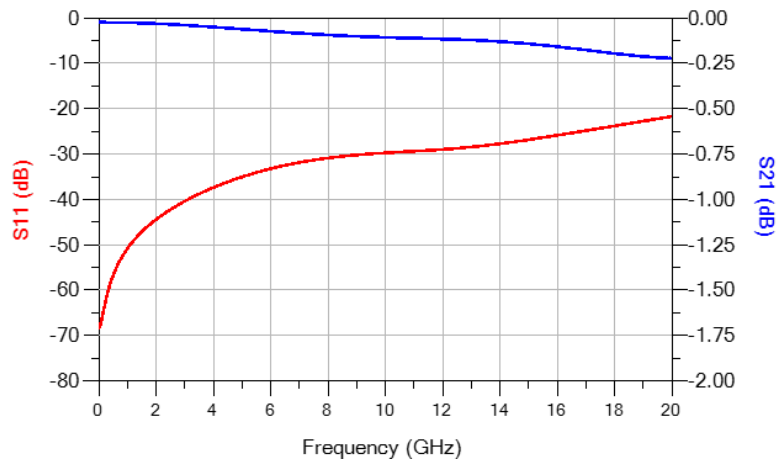


Figure 4.4 S-parameters of the tapered connector design

The DDM connector performs well through 20 GHz. However, the DDM receptacle must transition to a transmission line. The COTS adapter is designed to mate vertically with a female connector. In this case, the female connector is the DDM receptacle. Most applications require microstrip lines or another type of planar transmission line. The effects of transitioning from a vertical coaxial line to a horizontal microstrip is a challenge. In the next section, the design challenges and solutions will be discussed.

4.3 DDM Test Fixture Design

The DDM connector, without any transitions to a planar transmission line, shows good S-parameter performance. The connector maintains greater than 20 dB of return loss and less than 0.25 dB of insertion loss through 20 GHz (Figure 4.4). However, for many applications the need to transition to a planar transmission line arises. In this section, we will present the initial results of a vertical transition from the DDM connector to a microstrip line, optimization of a microstrip taper, and the optimization of an embedded semi-circular transition.

The test structure consists of two DDM connectors connected by a 50-ohm microstrip line (Figure 4.5). A 125 μm thick, 100% in-fill ABS ($\epsilon_r = 2.42$ $\tan\delta = 0.006$) substrate is used for the substrate. 50% in-fill ABS ($\epsilon_r = 1.6$ $\tan\delta = 0.003$) is used for the DDM connector, the effect of changing the dielectric is described further in the chapter. The microstrip line dimensions are calculated using linecalc and are shown in Figure 4.5b. The COTS adapter mates with the DDM receptacle with the signal pin contacting the inner conductor of the DDM receptacle. There is a missing ground to allow the via to make the connection with the microstrip line on the bottom side of the test fixture without shorting the signal pin to ground.

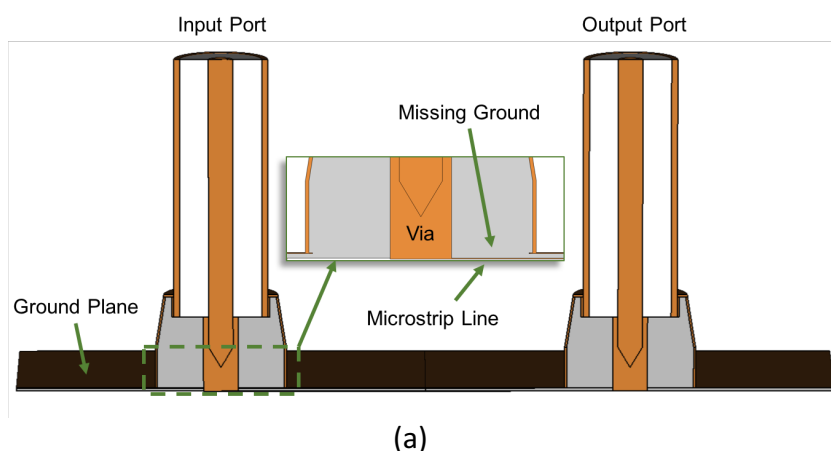
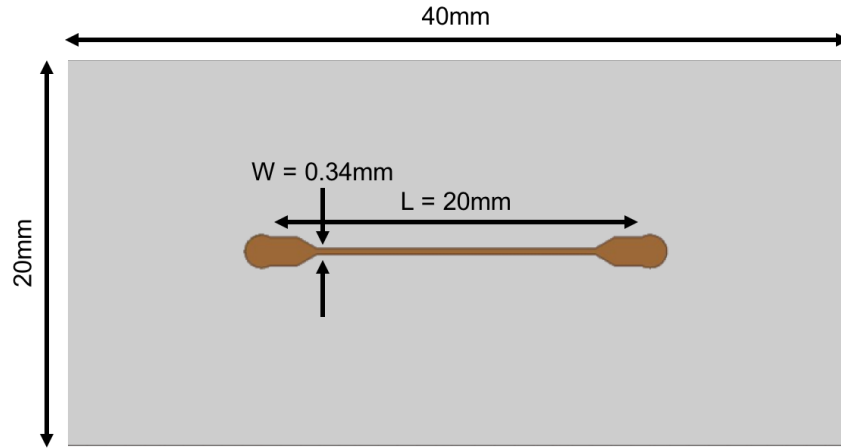


Figure 4.5 Simulation model of the DDM test fixture. (a) Cross-section of the DDM connector test fixture (b) Bottom view of the test structure showing the microstrip signal line



(b)

Figure 4.5 (Continued)

The simulation results for this circuit are shown in Figure 4.6. The test fixture performance cuts off around 4 GHz, which is well below the design requirement of 18 GHz. The cause of the degradation in performance is due to the discontinuity between the DDM connector and the microstrip line. The inductance at the discontinuity is large causing the impedance to increase significantly. Another cause of this impedance mismatch is the missing ground plane above the microstrip line, between the via and the outer conductor of the DDM connector; refer to the zoomed in view in Figure 4.5a.

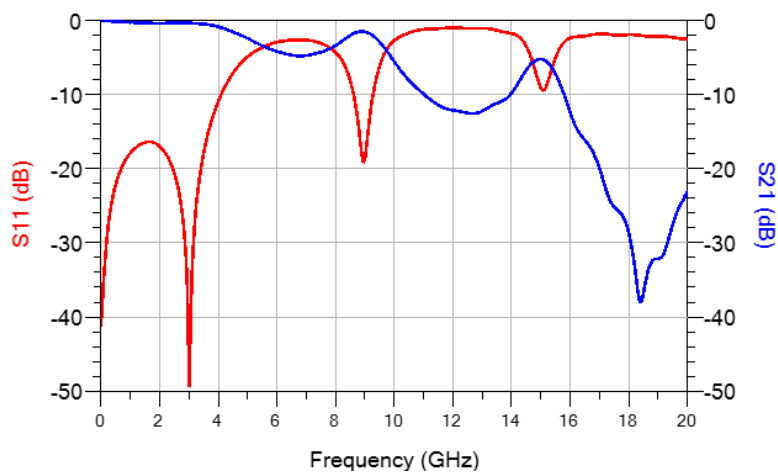


Figure 4.6 S-parameters of the initial test structure design

A few techniques can be used to reduce the inductance and discontinuity at the coaxial-microstrip interface. One solution would be to add a microstrip taper at the location where the coaxial signal line meets the microstrip line. Figure 4.7 shows a TDR plot as the taper width is swept from 0.5 mm to 1.5 mm.

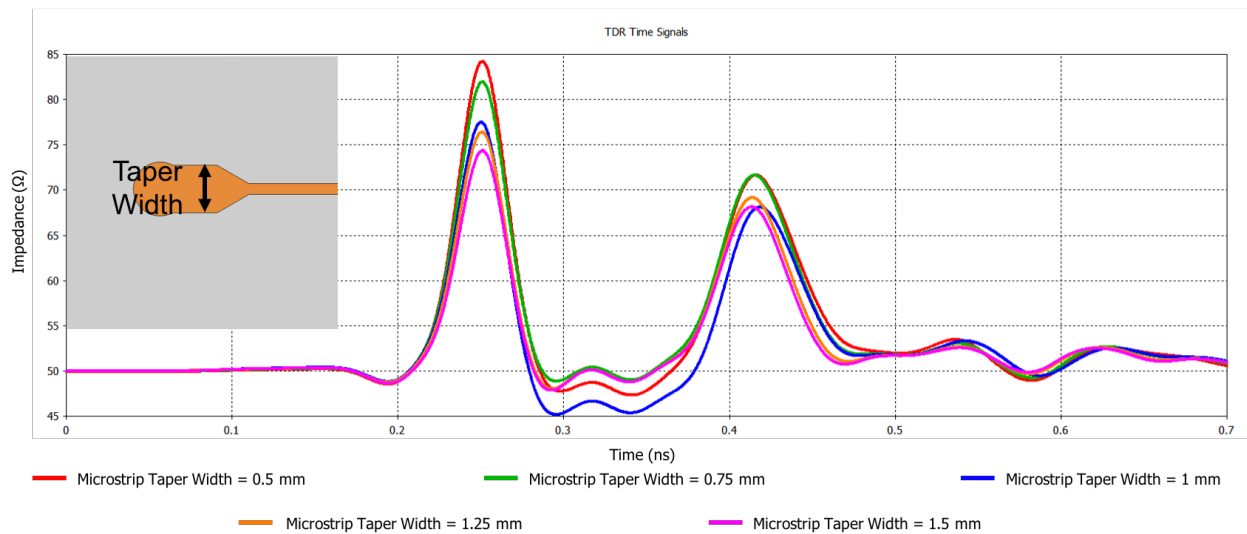
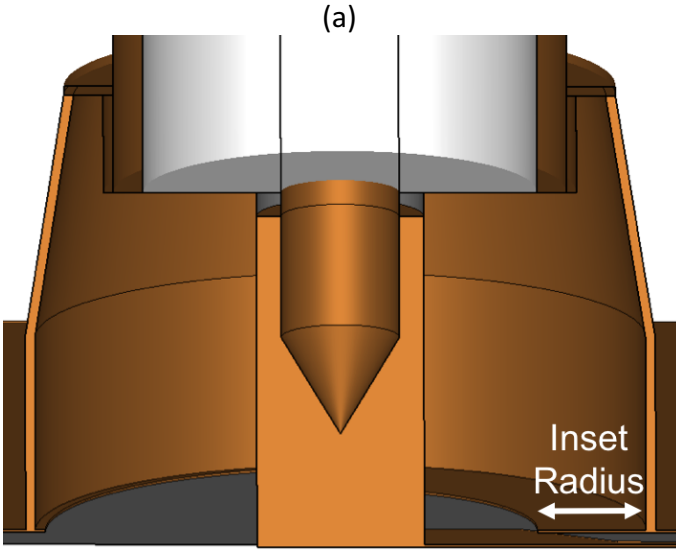
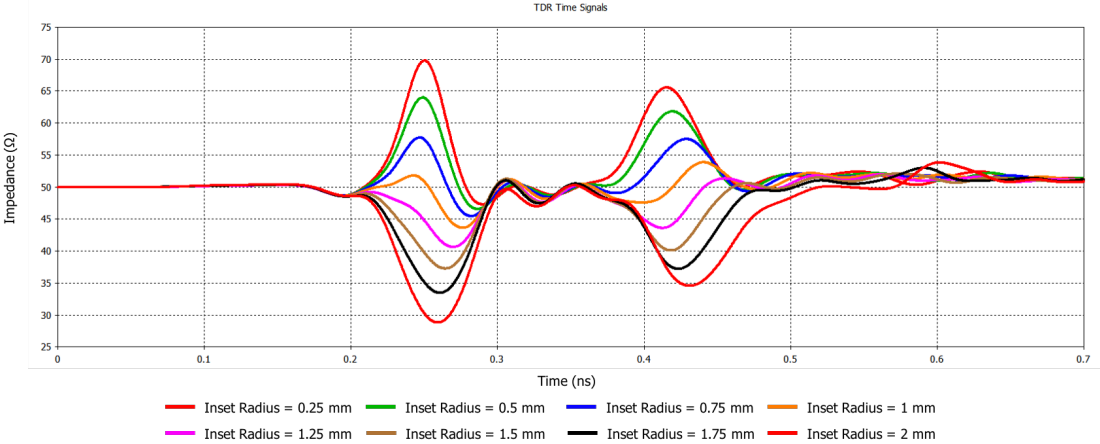


Figure 4.7 TDR plot of changes in taper width

The taper does help with the impedance mismatch, however by itself the taper cannot sufficiently reduce the inductance at the discontinuity. To further reduce the inductance, the ground plane at the coaxial-microstrip boundary needs to be brought closer to the coaxial signal line. This change will increase the capacitance of the microstrip line, effectively reducing the impedance. Figure 4.8a shows the TDR results of a parameter sweep which insets the ground closer to the signal line of the DDM connector. Figure 4.8b shows how the ground is inset in a semicircular fashion. The inset radius is the distance from the outside of the connector towards the signal line. The TDR shows that the 1 mm inset radius offers the best impedance match along the line. However, this is deceiving without looking at the S-parameters. Figure 4.9 shows the insertion loss and return loss of the test fixture when the DDM connector has a 1 mm inset radius.

Even though the impedance match is reasonable the added structure is causing the E-field from the DDM connector to abruptly change to the E-field configuration of the microstrip.



(a)
 (b)
 Figure 4.8 Simulation results and model varying the inset radius.
 (a) TDR Plot varying the inset radius (b) 3D model including the inset ground

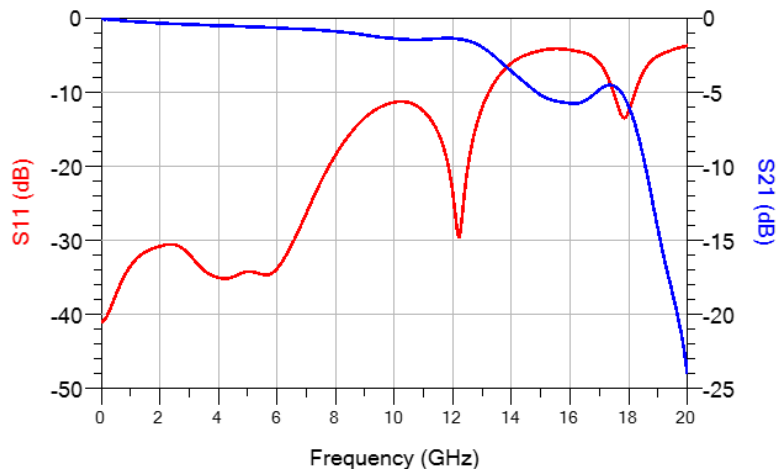


Figure 4.9 S-parameters of the DDM test structure with an inset radius of 1 mm

Even though the characteristic impedance is matched, it is important that the E-field configuration is also converted effectively between the different transmission line types [20]. Figure 4.10 shows the E-field at the transition. At the transition point of the DDM connector, the E-fields change their orientation by 90° to transition to the microstrip line. It can be shown that if the inset ground is angled upwards into a semicircular cone, it will provide a ground section that will allow the E-fields to gradually transition from a horizontal orientation to a vertical orientation.

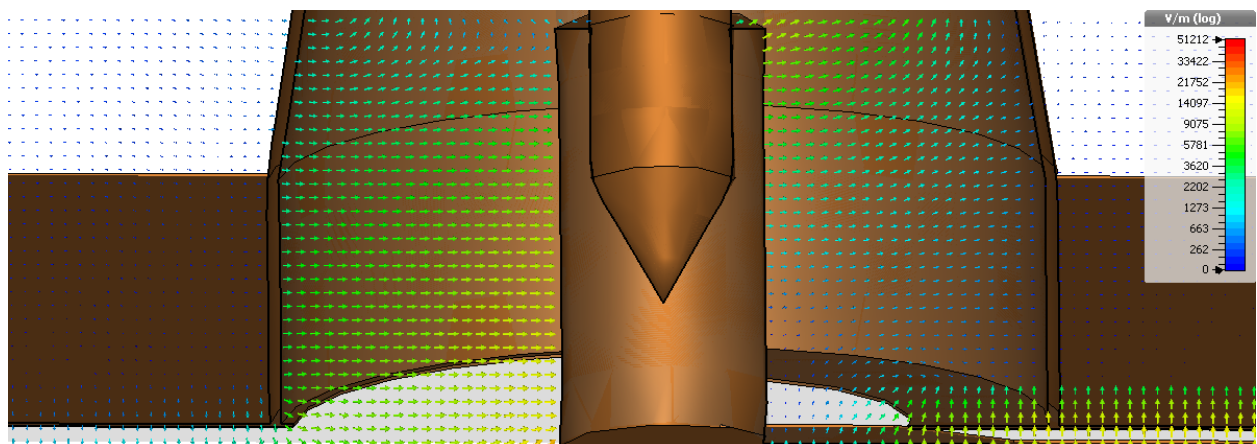


Figure 4.10 Electric field configuration inside the DDM connector at the DDM-microstrip transition

The inset ground is transformed into a cone with a height of 0.4 mm and an inset of 1 mm as shown in Figure 4.11. A parameter sweep of the semi-circular cone radius is performed. The TDR and S-parameters of the sweep are shown in Figure 4.12.

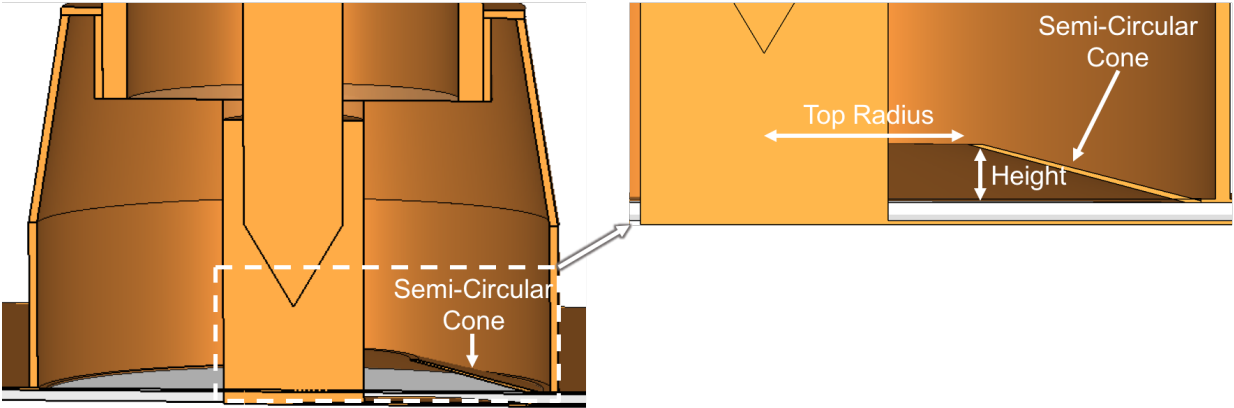
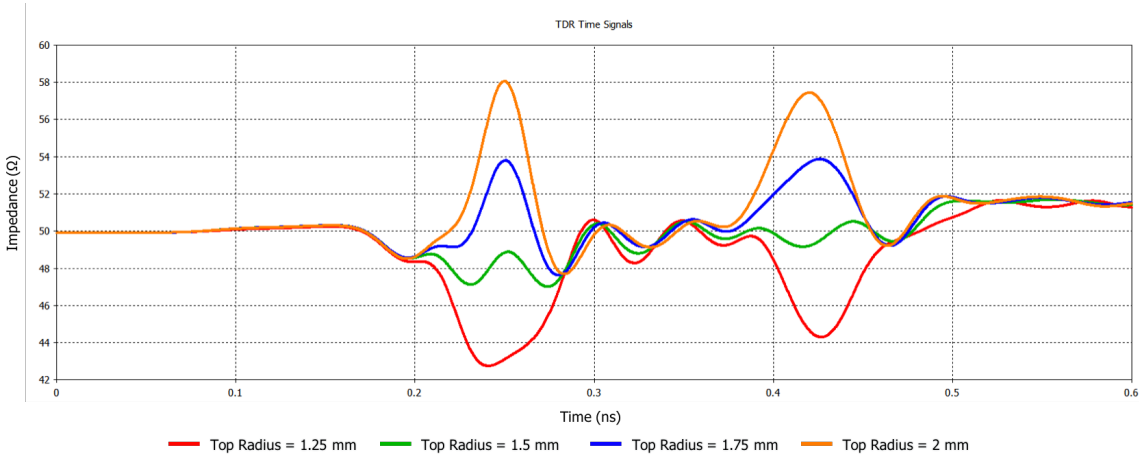


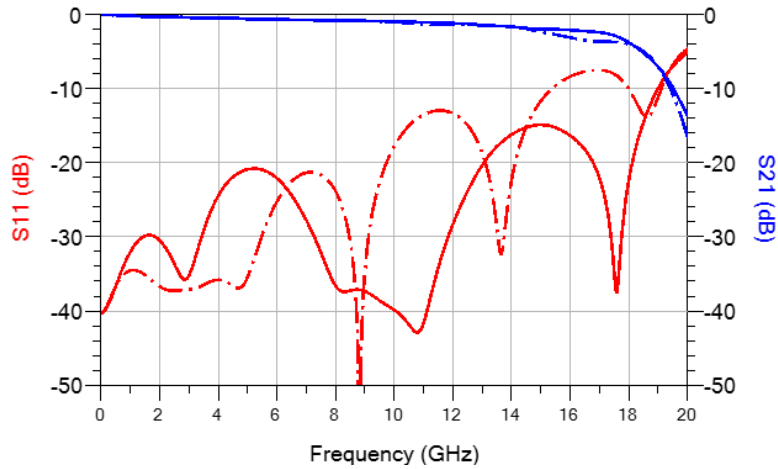
Figure 4.11 DDM model with the semi-circular cone transition added within the structure

A TDR analysis shows that the impedance is matched closest when the Top Radius is 1.5 mm. The S-parameters with a Top Radius of 1.5 mm provides more than 10 dB of return loss up to 19 GHz.



(a)

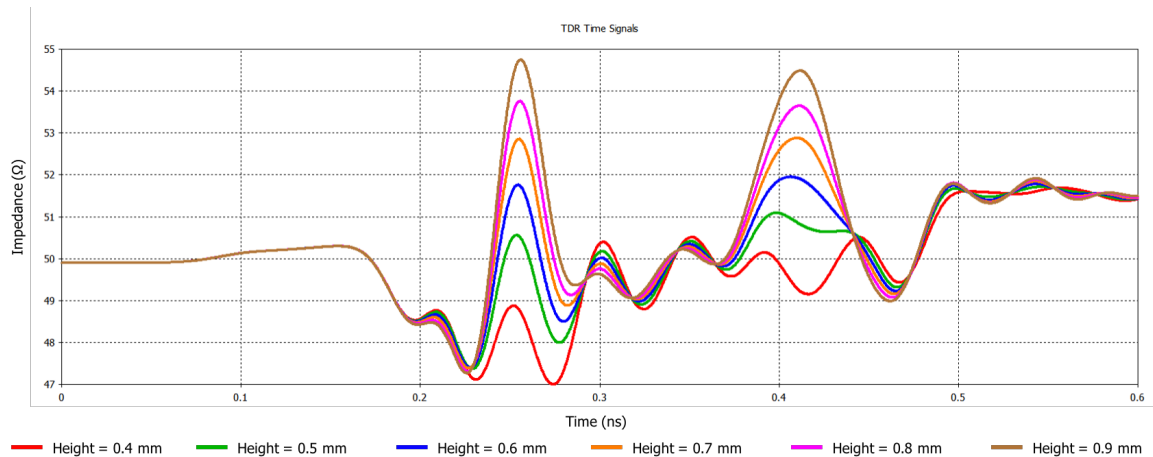
Figure 4.12 DDM test fixture simulation results varying the transition radius. (a) TDR plot (b) S-parameters of the semi-circular transition (via offset = 0.25 mm top taper = 0.4 mm microstrip taper width = 1.5 mm transition height = 0.4 mm) dashed line – 1.75 mm, solid line – 1.5 mm



(b)

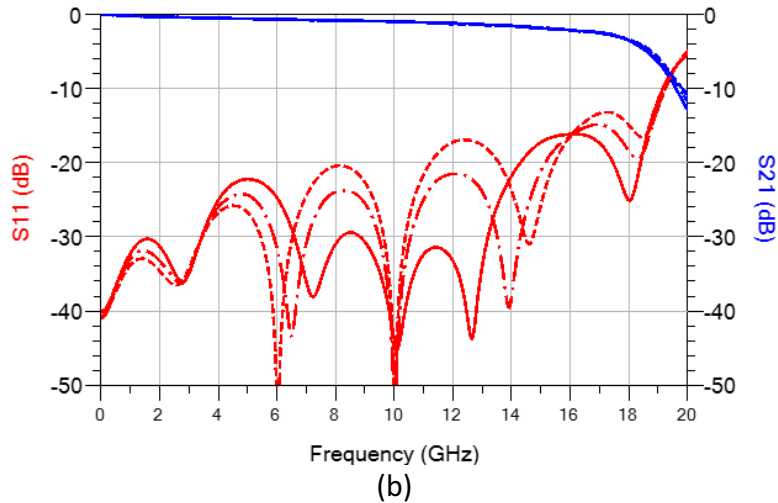
Figure 4.12 (Continued)

Keeping the Top Radius parameter constant at 1.5 mm the height parameter can be swept. The TDR and S-parameter plots are shown in Figure 4.13. The S-parameters for 0.5 mm, 0.6 mm and 0.7 mm are shown for comparison. It is observed from the TDR plot that the impedance increases with the height parameter. The semi-circular ramp equalizes the impedance at the discontinuity to approximately 50 ohms.



(a)

Figure 4.13 DDM test fixture simulation results varying the transition height. (a) TDR plot (b) S-parameters of the semi-circular transition (via offset = 0.25 mm top taper = 0.4 mm microstrip taper width = 1.5 mm top radius = 1.5 mm)
Solid – 0.5 mm Dash-Dot – 0.6 mm Dash – 0.7 mm



(b)
Figure 4.13 (Continued)

The S-parameter data show that the change in height mainly affects mid-band parameters. Figure 4.14 shows the E-field configuration with the optimized (top radius = 1.5 mm and transition height = 0.6 mm) semi-circular transition. The S-parameters in Figures 4.12b and 4.13b show that no changes in the transition height or radius will extend the operating frequency of the test fixture. This is due to the introduction of the TE_{11} mode within the DDM connector. The cut-off frequency for the DDM connector can be calculated using Equation 4.3 [11], where d is the outer diameter of the inner conductor and D is the inner diameter of the outer conductor. Two dielectric constants are possible by changing the in-fill percentage of the ABS within the DDM connector, $\epsilon_r = 1.6$ (50% in-fill) and $\epsilon_r = 2.4$ (100% in-fill). Using the actual dimensions of the connector ($D = 6.2$ mm and $d = 2$ mm) the predicted cut-off frequencies assuming $\epsilon_r = 1.6$ and $\epsilon_r = 2.4$ are 18 GHz and 14.5 GHz, respectively. These predicted cut-off frequencies do not match the simulation results, however, because the radius isn't constant when considering the embedded transition. The value for the inner diameter of the outer conductor is smaller. If a diameter is chosen close to the average value, $D = 4.5$ mm, then $f_c \approx 23$ GHz for $\epsilon_r = 1.6$ and $f_c \approx 19$ GHz for $\epsilon_r = 2.4$, which is closer to the simulated result in Figure 4.15.

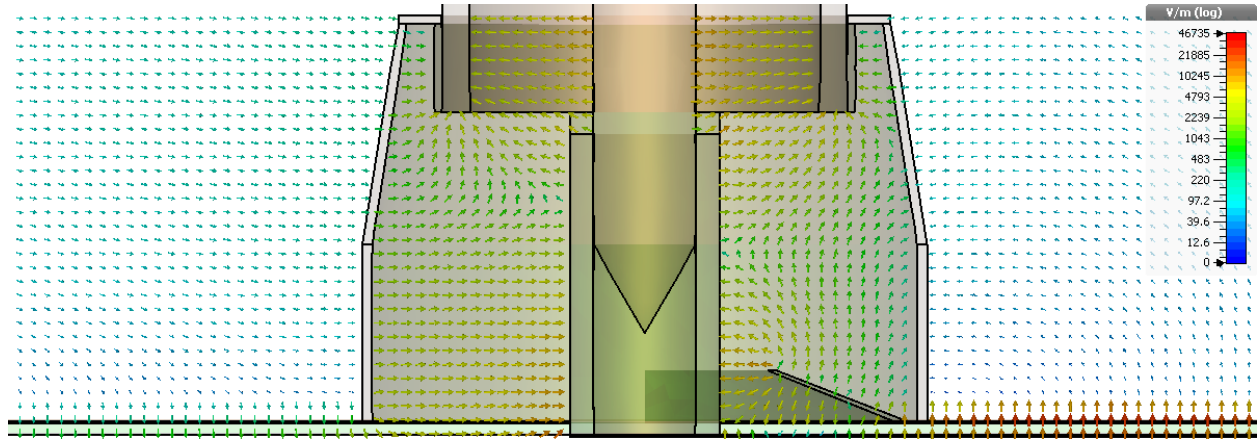


Figure 4.14 Electric field configuration of the DDM connector with the optimized transition

$$f_c = \frac{2C_0}{\pi(d+D)\sqrt{\epsilon_r}} \quad (4.3)$$

One way to increase the operating frequency of the DDM connector is to reduce the dielectric constant. This will increase the TE₁₁ mode cutoff frequency. An S-parameter comparison between the DDM connector with a dielectric constant of 2.4 and 1.6 is shown in Figure 4.15.

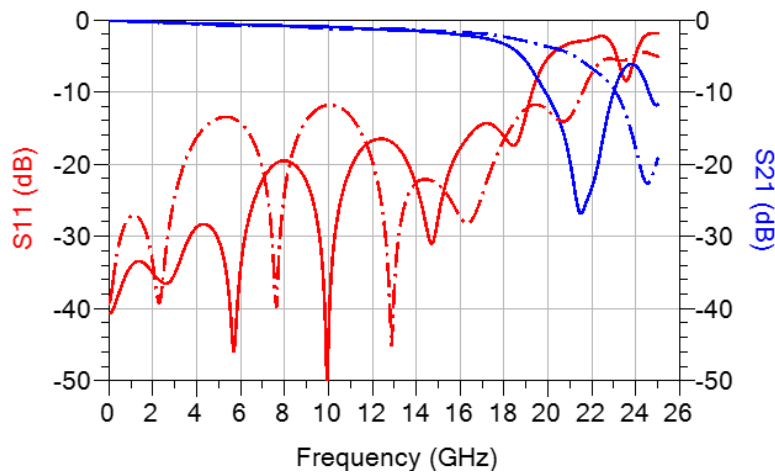


Figure 4.15 S-parameters of the structure with different dielectric constants.
Solid – 2.4 Dash-Dot – 1.6

4.4 Design Considerations

Manufacturing technology limitations and processes need to be considered when designing any structure, RF or otherwise, and DDM is no exception. Considerations include layer print order as well as vertical conductor printing. When designing DDM connectors these matters need to be addressed.

When considering the print order of the connector test fixture it is quickly realized that the current form is not printable. Figure 4.16 helps demonstrate the issues with the printability of the current design. If the microstrip line is printed first the conductor would be printed on the heated print bed.

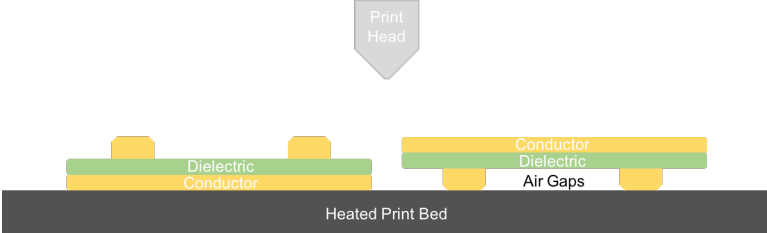


Figure 4.16 Different printing orientations to demonstrate the issues with printing the DDM connector test fixture

If the DDM connector is printed first, then there would be air gaps and it will not be possible to print the rest of the circuit. A support structure could be used to solve this issue. However, due to the thin substrate, removing the supports would likely damage the test fixture. These issues can be resolved by first printing a small layer of ABS (Figure 4.17).

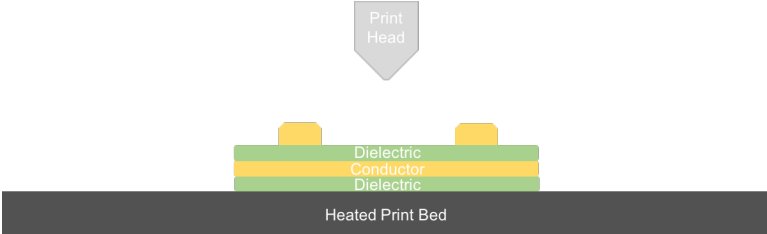


Figure 4.17 Modification required to successfully print the test structure

Adding a 0.1 mm print layer does change the performance of the connector test fixture. The largest change occurs at 18 GHz with an increase of insertion loss of approximately 0.5 dB. However, the return loss remains greater than 10 dB through 18 GHz (Figure 4.18).

Vias are a significant challenge with the CB028 printing process, and vertical printing is not currently possible. Since the vias cannot be printed, the via offset will be removed. Filling the via by-hand isn't accurate enough to guarantee a 0.25mm via offset.

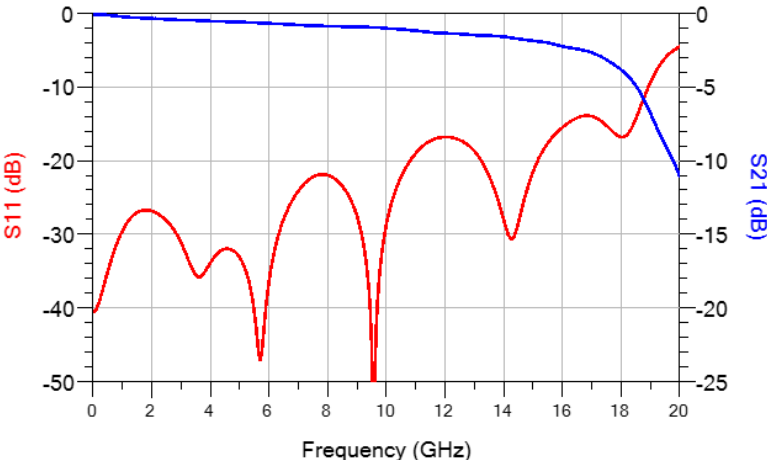


Figure 4.18 S-parameters of the test structure with the 0.1 mm print layer added

The S-parameter results of the test fixture with and without a via offset, from Figure 4.3, are shown in Figure 4.19. As mentioned in Section 4.2, the via offset has an impact on the impedance match at the COTS-DDM connector interface. The change in the via offset reduces the return loss at mid-band frequencies and increases the return loss at the upper frequencies. The change in the offset length has no effect on the insertion loss of the design.

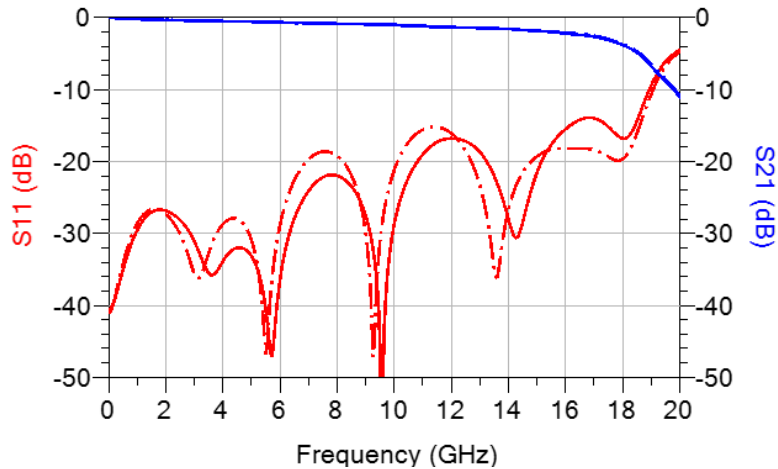


Figure 4.19 S-parameters of the test structure with the modified via offset.
 Solid – Via offset Dash-Dot – No via offset

A final consideration of the design is the mechanical structure needed to prevent the COTS adapter from shifting and preventing strains/stresses on the DDM connector. To address this concern, a 100% infill ABS structure is designed to act as a receptacle for the COTS adapter. The structure is added to the simulation to ensure that there are no performance degradations. Figure 4.20 shows the final design and the S-parameter results comparing the simulation results with and without the mechanical structure.

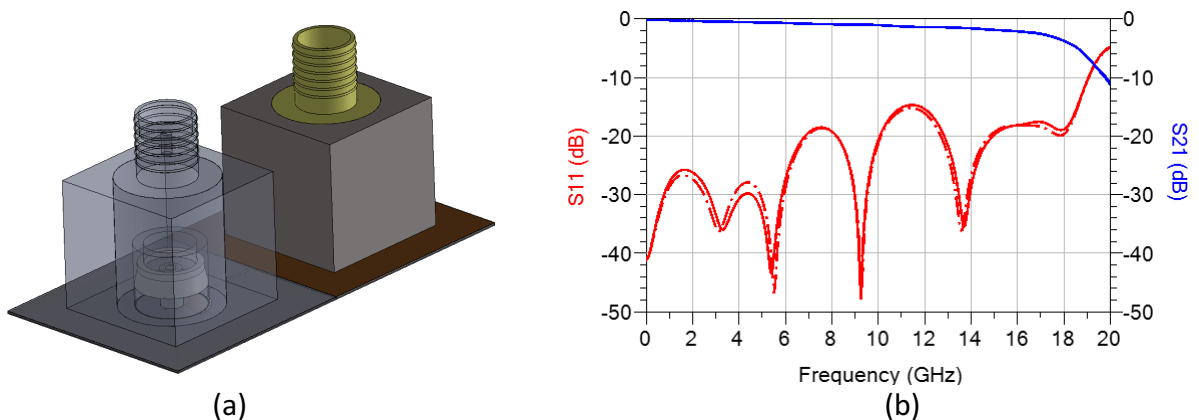


Figure 4.20 Model and simulation data of the test structure with and without the mechanical structure. (a) 3D model (b) S-parameters
 Solid – Mechanical Structure Dash-Dot – No Mechanical Structure

4.5 Simulation vs Measurement Results

The previous sections discussed the general design process of the connector design. In this section, the simulated and measured results will be compared. A cross section of the fabricated design is shown in Figure 4.21 along with a picture of the fabricated structure without the mechanical structure or COTS adapters attached.

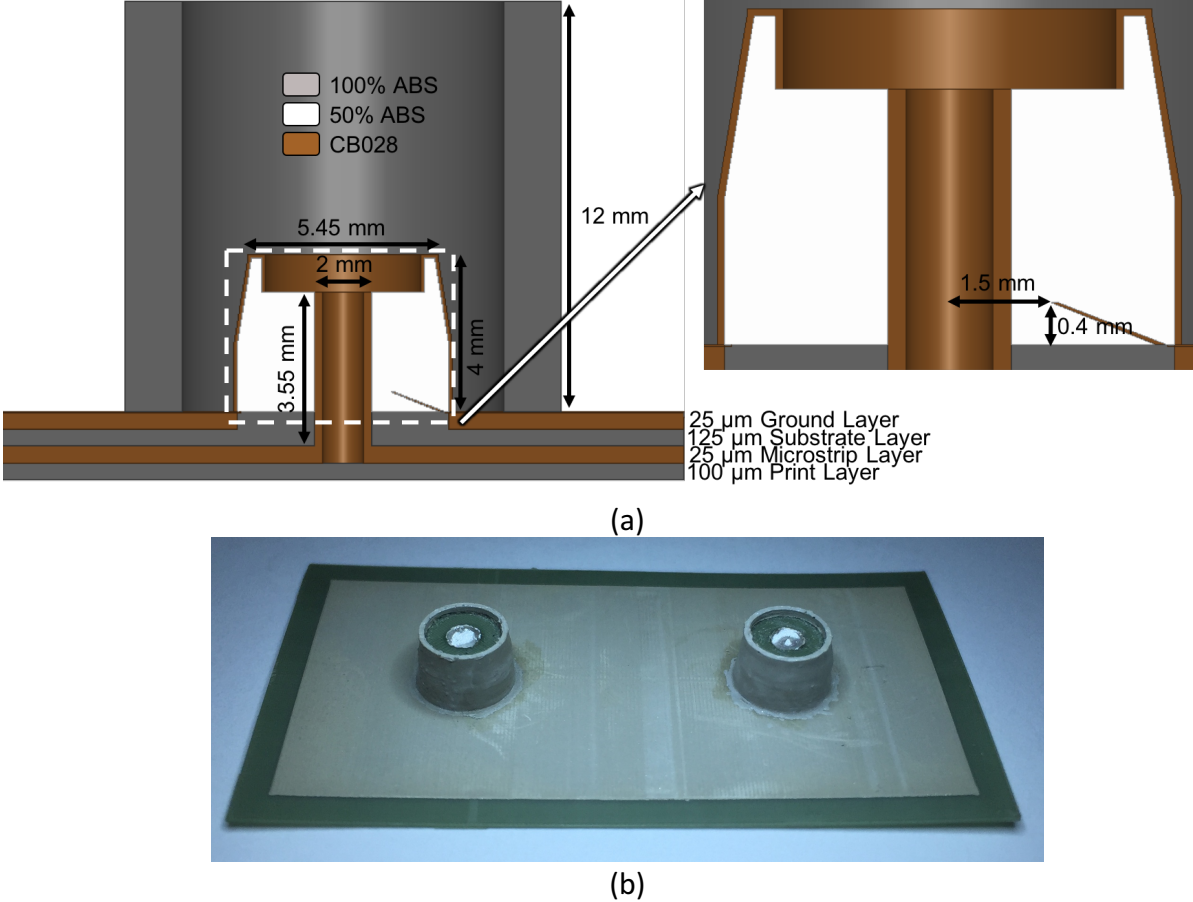


Figure 4.21 3D model and fabricated DDM test fixture.
 (a) Illustration of fabricated connector model (b) 3D printed structure

The connector fixture is measured with its reference planes set at the COTS adapter input, not the DDM connector input. A Keysight PNA-X was used to measure the structure with the calibration being conducted using a Keysight 85052B 3.5 mm calibration kit. The measured and simulated results are shown in Figure 4.22. The measurement data doesn't show very good

correlation with the simulated data beyond 14 GHz. The return loss through 14 GHz is greater than 12 dB and the insertion loss is less than 2.92 dB. The insertion loss of the measurement data increases substantially at 15 GHz, which isn't predicted in the simulation. The COTS adapter is de-embedded and the losses of the microstrip are removed. The resulting insertion loss of the DDM connector is 0.45 dB.

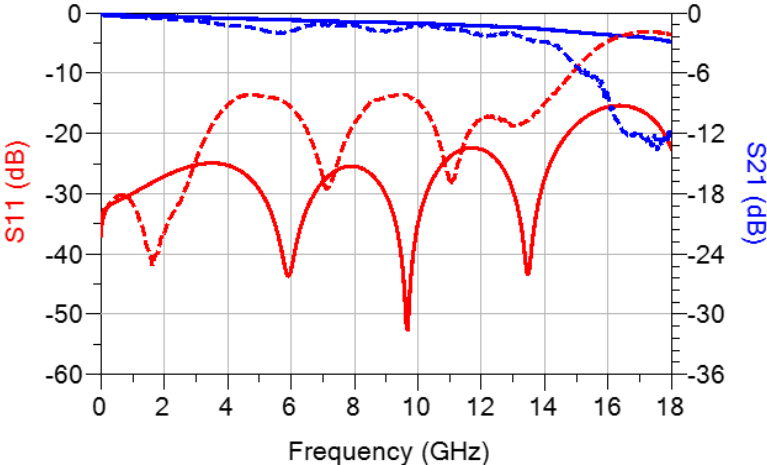


Figure 4.22 Measured vs simulated S-parameter data of the test structure.
 Solid – Simulated Dashed – Measured

The measurement suggests that TE_{11} cutoff is being shifted to a lower frequency. The two likely causes were either dielectric constant changes or structural issues, or a combination of both. The easiest issue to check is the transition within the connector. This is the easiest due to the fragile nature of the DDM connector and the ease with which it can be separated from the connector at the transition. Upon removal of the DDM connector from the substrate, with the transition exposed, it appears that the printed transition wasn't completely continuous (Figure 4.23). This could be due to the subsequent ABS layer printing or the conductor printing itself. The CB028 gap was introduced into the DDM connector model as well as an ABS transition as shown in Figure 4.23. If the transition was not damaged there would be no gaps in the CB028 semi-

circular transition (Figure 4.23a). The gap in Figure 4.23b is only introduced to model the damaged transition in Figure 4.23a.

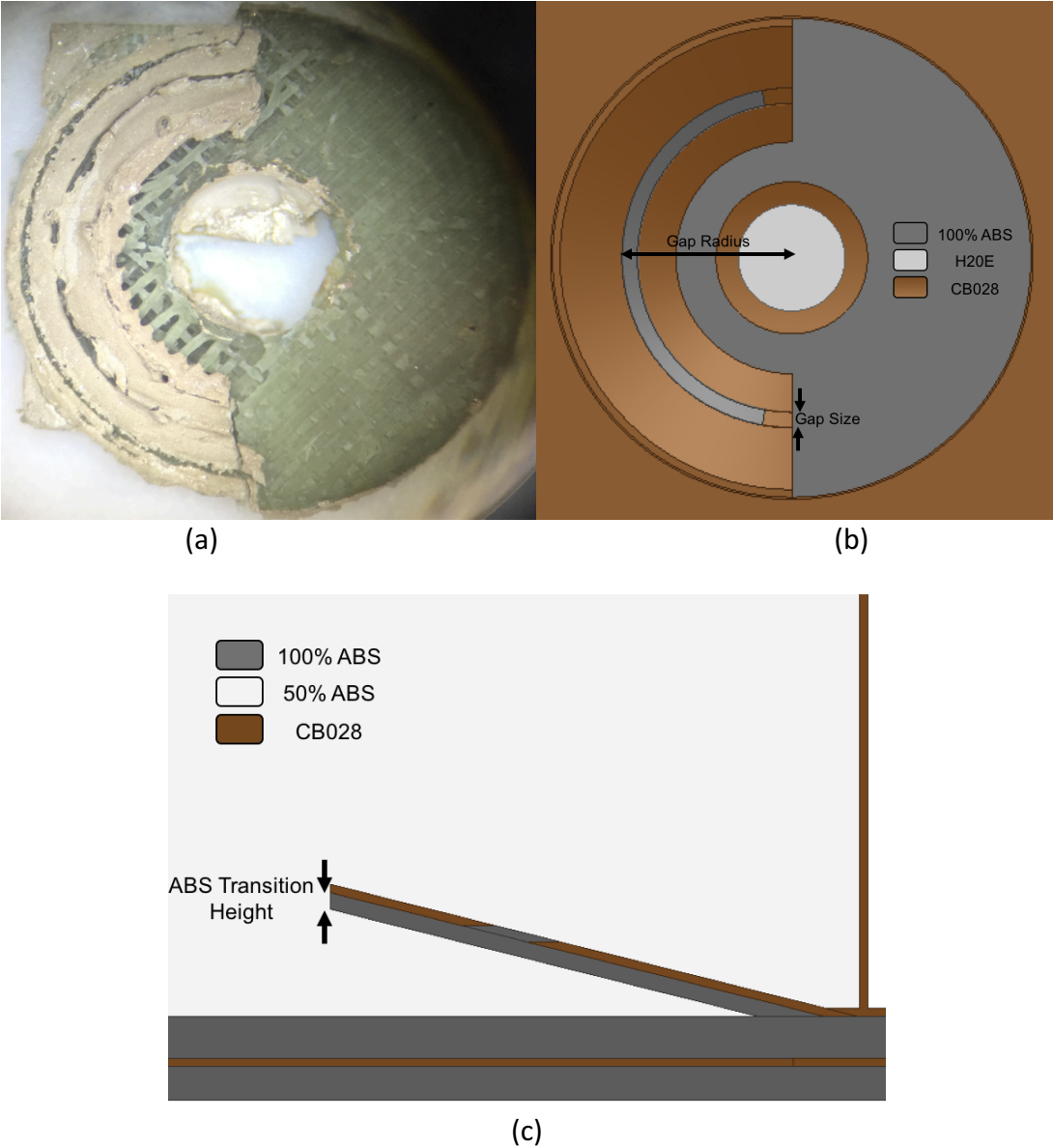


Figure 4.23 Fabricated and 3D model of damaged transition. (a) Photo of the semicircular transition (b) 3D model of the modified transition accounting for the conductor gap (c) DDM embedded transition with an ABS transition height added

Three parameters are introduced: Gap Radius, Gap Size, and ABS Transition Height. The ABS transition is introduced to simulate the possible change in the dielectric due to the printing of the transition. Parameter sweeps are performed by not only varying the above parameters but

also by including the modified transition in just one and both DDM connectors. A parameter sweep is performed with the modified transition included in only one of the DDM connectors. The ABS transition height is varied while holding the gap radius constant (Figure 4.24). The two gap sizes are also shown in the Figure 4.24. Figure 4.24 shows that varying the ABS transition height alone is not enough to lower the cutoff frequency. Changing the gap size does not shift the S_{21} resonance significantly. However, it does have a significant impact on the losses at the resonance.

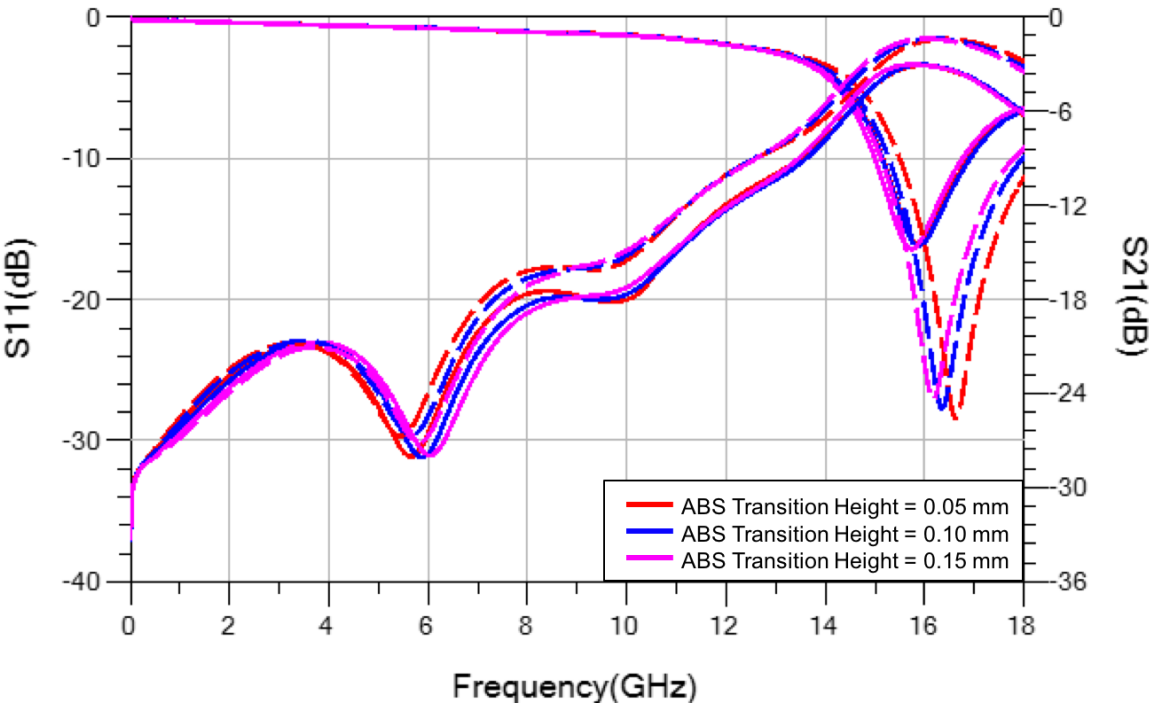


Figure 4.24 S-parameter sweep of the ABS transition height with one connector damaged.
 Gap Radius: 2.3 mm
 Solid – Gap Size: 0.025 mm, Dashed – Gap Size: 0.05 mm

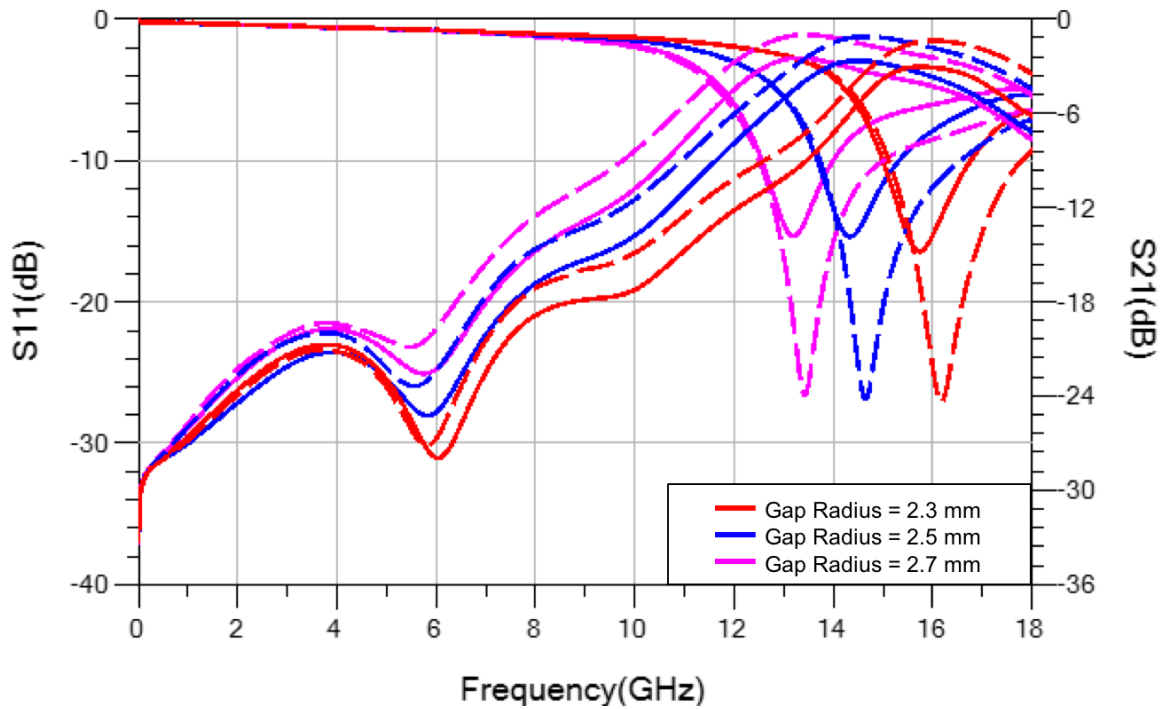


Figure 4.25 S-parameter sweep of the gap radius with one connector damaged.
 ABS Transition Height: 0.15 mm
 Solid – Gap Size: 0.025 mm, Dashed – Gap Size: 0.05 mm

Figure 4.25 is a parameter sweep of the gap radius while keeping the ABS transition height constant. It can be seen that the gap radius contributes greatly to the shift in the resonance frequency. Changing the gap radius by 0.2 mm causes a shift in the resonance frequency by more than 1 GHz. This significant change is enough evidence to show that the change in the measurement data vs simulation data is due to the position of the conductor gap. However, there is the possibility that the conductor gap is occurring in both of the DDM connectors.

The conductor gap is included in both DDM connectors and the same parameter sweeps are performed. As expected the addition of another conductor gap causes greater disruption in the losses across the whole frequency band. Figure 4.26 shows the simulated results of the DDM connector structure while varying the ABS transition height. The ABS transition height does affect the losses but again it is not enough to change the resonance frequency alone.

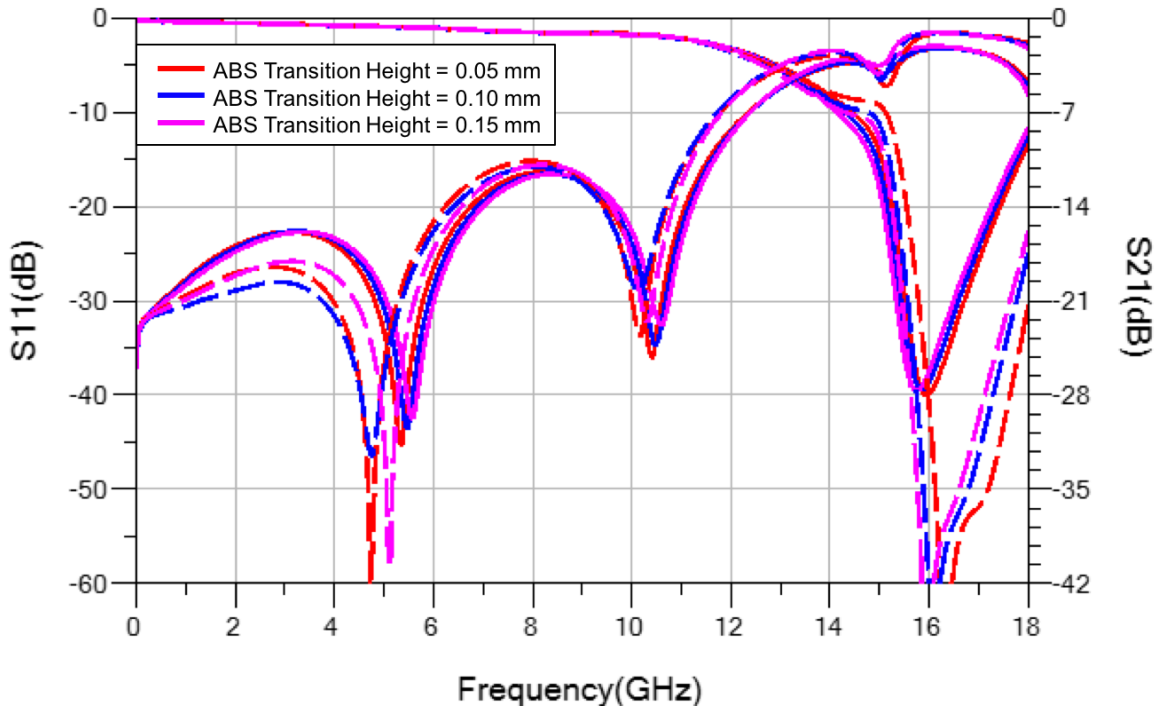


Figure 4.26 S-parameter sweep of the ABS transition height with both connectors damaged.
 Gap Radius: 2.3 mm
 Solid – Gap Size: 0.025 mm, Dashed – Gap Size: 0.05 mm

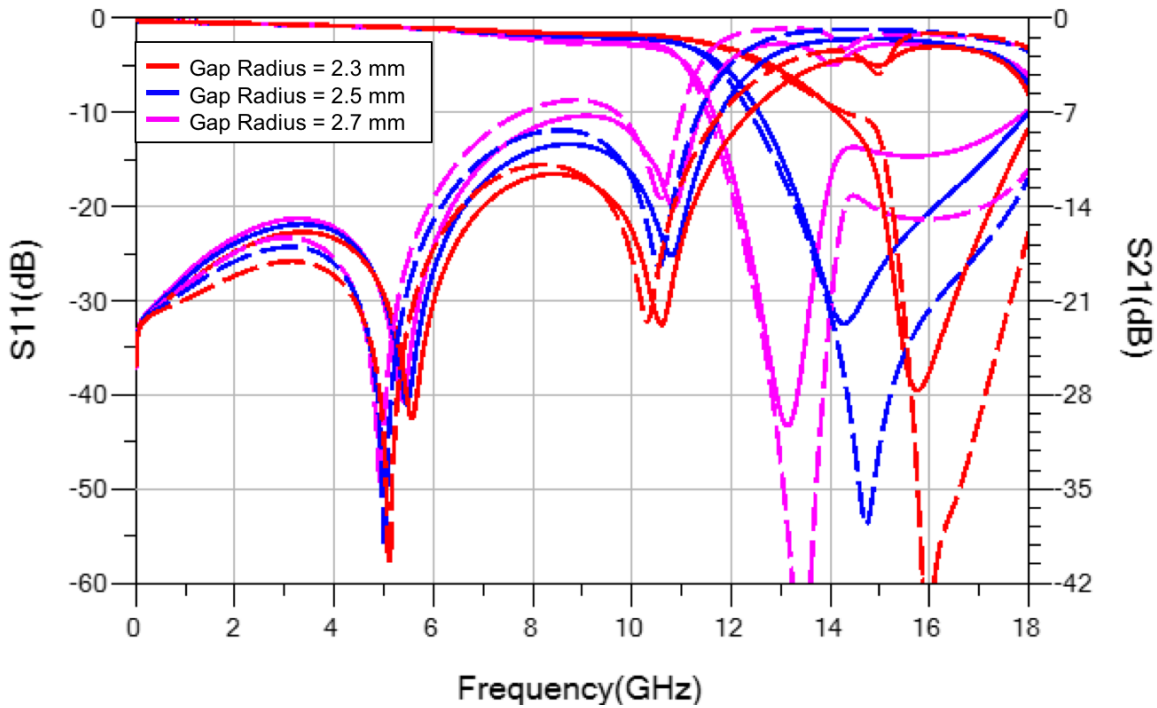


Figure 4.27 S-parameter sweep of the gap radius with both connectors damaged.
 ABS Transition Height: 0.15 mm
 Solid – Gap Size: 0.025 mm, Dashed – Gap Size: 0.05 mm

Figure 4.27 shows the simulated performance while varying the gap radius. The S_{21} resonance at each gap radius is consistent with the case where only one modified DDM connector is included. The main difference between one and two modified connectors is the mismatch across the band.

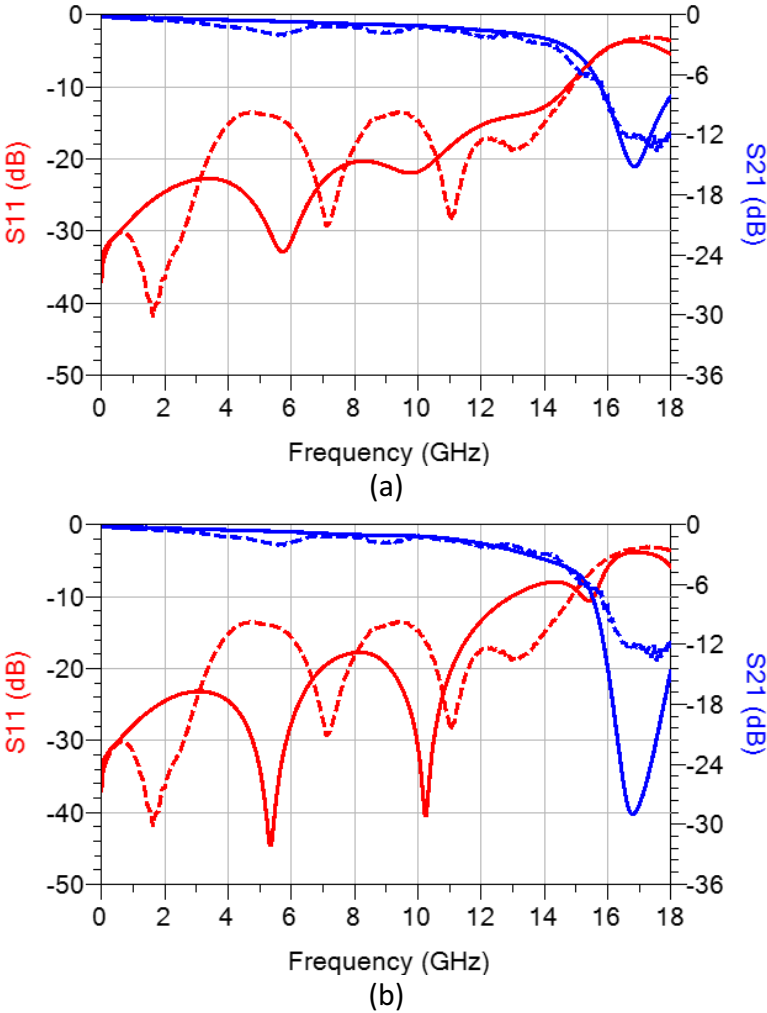


Figure 4.28 S-parameter data of the DDM test fixture with a damaged connector.
 (a) one modified transition (b) two modified transitions
 Solid – Simulated, Dashed – Measured

The combination that results from the above analysis are a gap size of 25 μm and a radius of 2 mm. However, depending on the combination of the conductor gap width, conductor gap radius and the thickness of the ABS transition, similar results can be attained. Figure 4.28 shows

the simulation results of the modified DDM connector transition with only one transition modified (a) and both transitions modified (b). The simulation with one connector modified matches the measurement data closer than the DDM connector with both transitions modified.

4.6 Transition Modeling

In the previous sections, the connector structure was modeled using a 3D electromagnetic solver. However, it is also useful to create a lumped component model of the connector structure. When modeling any component, it is beneficial to start at the basic model to get an approximation of the behavior of the circuit. Connectors and transmission lines are no exception. Figure 4.29 shows the lumped-element equivalent circuit model for a transmission line with which the connector can be modeled. All TEM transmission lines can be modeled using this configuration. The determination of the lumped components is covered in many textbooks to include [11]. The DDM connector from Section 4.5 is determined to have a transitional issue where there is a gap in the transition conductor. This gap is causing the second dominant mode, TE_{11} , to propagate in the desired operating band. Here its shown that by creating a lumped component model, it is possible to represent the issue in another form.

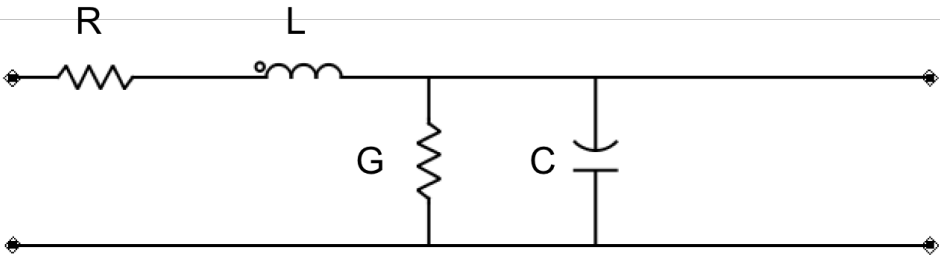


Figure 4.29 Lumped component model for a transmission line

The schematic in Figure 4.30 shows the overall circuit for the connector test fixture shown in Figure 4.20. There is good agreement between the 3D model and the lumped component model S-parameters (Figure 4.31). The phase of S_{21} for both models also match well.

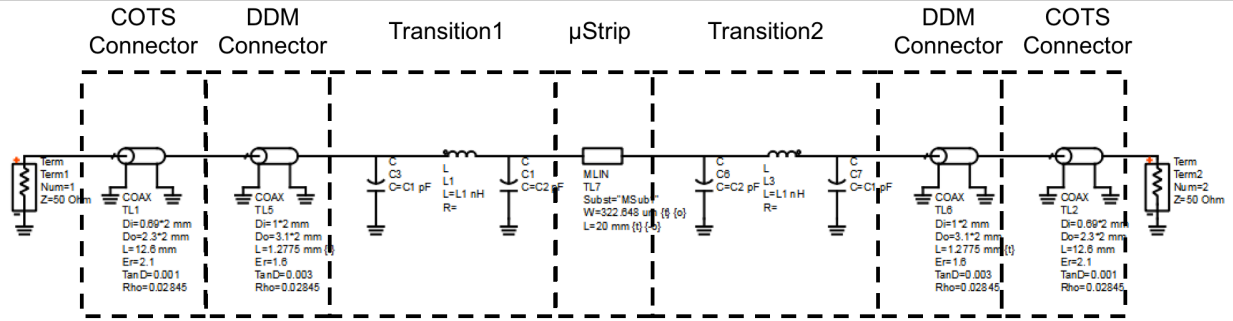
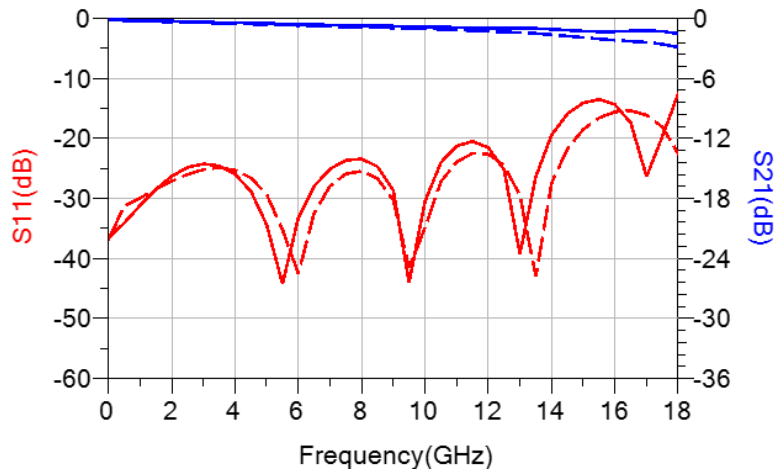
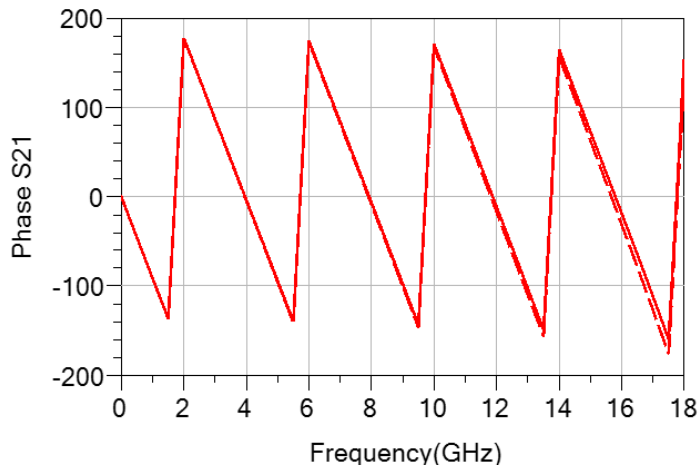


Figure 4.30 Lumped component model of the test structure without the modified transition



(a)



(b)

Figure 4.31 Performance of the lumped component model without a modified transition.

(a) S-parameters (b) Phase

Solid – Lumped Component Model, Dashed – 3D Model

The model is modified as shown in Figure 4.32, to emulate the measurement data of the damaged connector. The capacitor across the inductor is added to model the conductor gap of the measured connector. The shunt capacitances are also varied instead to accurately represent the modified transition. Comparisons of the measured and simulated S-parameters are shown in Figure 4.33. The parallel capacitor is related to the transition height and radius. For example, as the capacitance value is increased this has the same effect as increasing the radius of the transition. Increasing the transition radius shifts the resonance lower in frequency, as does increasing the capacitance.

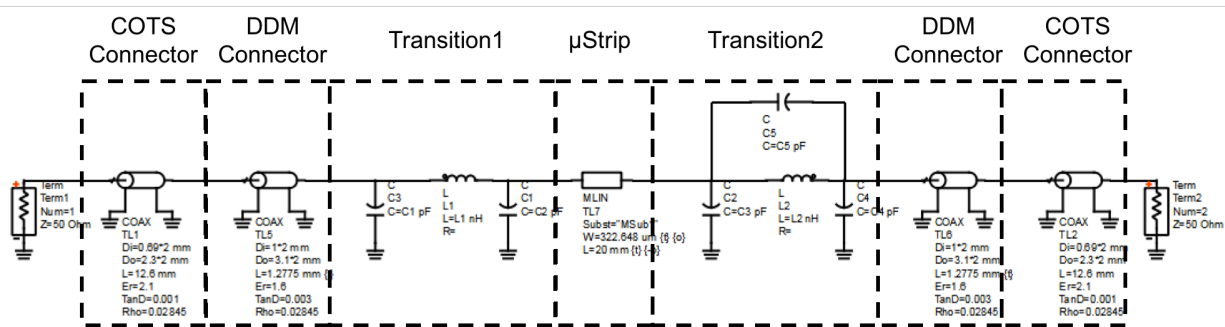


Figure 4.32 Lumped component model of the test structure with the modified transition

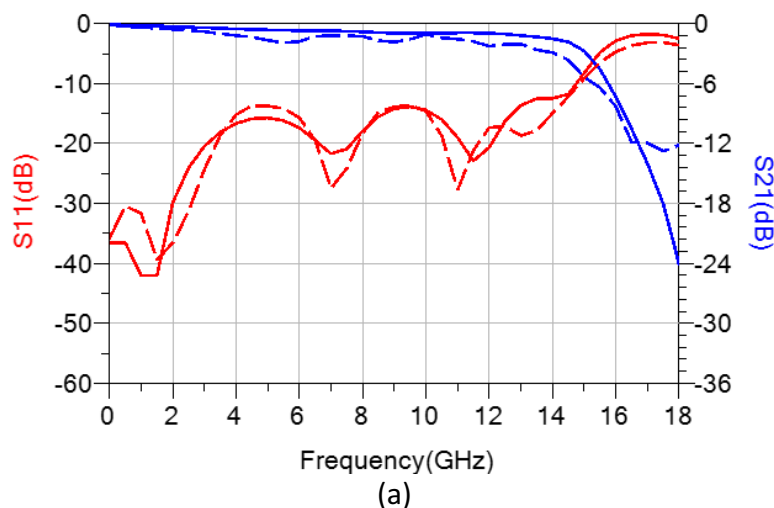


Figure 4.33 Performance of the lumped component model with a modified transition.
 (a) S_{11} and S_{21} Magnitude (b) S_{21} Phase
 Solid – Simulated, Dashed – Measured

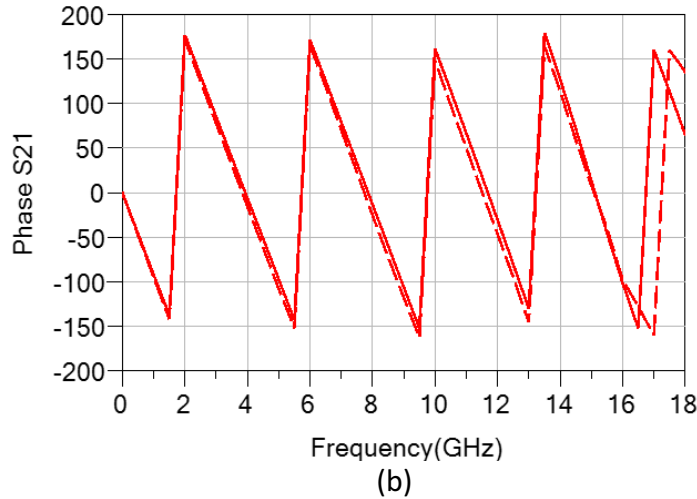


Figure 4.33 (Continued)

4.7 Conclusion

The connector design process requires many steps and special attention when utilizing additive manufacturing processes. Utilizing the TDR tool enables the designer to locate points of a discontinuity within a circuit. Impedance is an important consideration; however, the electric field configuration is just as crucial when designing a good transition/connector. Manufacturing considerations need to be addressed when utilizing DDM including: print order and printing limitations. Electromagnetic simulators are invaluable tools that allow designers to troubleshoot discrepancies between simulated and measured data. A lumped component model was developed and proved useful in validating physical defects in the connector prototypes.

CHAPTER 5: DDM THERMAL MANAGEMENT

5.1 Introduction

Effective thermal management is paramount for high power and high reliability applications. High heat applications utilize multiple thermal management systems including: heat spreaders, heat sinks, and air cooling, to name a few [21]. The challenge in 3D printing is that thermoplastics are inherently insulators with low thermal conductivities, making it difficult to effectively remove heat from a system. Common thermoplastics such as ABS and polylactic acid (PLA) have glass transition temperatures below 110°C. There are higher temperature thermoplastics such as the Stratasys UTLEM family, which is polyetherimide (PEI). However, the higher temperature could cause issues in the FDM printing process. In section 5.2, we will discuss a few thermal definitions to understand the work in section 5.4. In section 5.3, we will discuss the thermal and RF measurements of a Ku-band power amplifier (PA). In section 5.4, a thermal model is discussed to determine how to overcome the challenges of a PA on thermoplastics.

5.2 Thermal Background

Three heat transfer modes are possible: conduction, convection and radiation. In this work, only conduction and convection are considered. Conduction is the transfer of heat across a stationary solid or fluid. Convection is the transfer of heat from a surface to a moving medium [22]. Conduction is important in the analysis of the PA test fixture because it is the main thermal transfer method. The heat is generated on the die of the PA and travels to the ground pad of the

package. From there it is attached to a PCB where thermal vias transfer the heat to the brass carrier. Fourier’s law is the rate equation used for heat transfer. Fourier’s law is expressed as:

$$q_z'' = -k \frac{dT}{dz} \tag{5.1}$$

where k is the thermal conductivity, T is the temperature and q is the heat flux [22]. K is an important material property that describes how well a material can transfer heat. ABS has a thermal conductivity of 0.22 W/m·K which means it is ineffective at transferring heat through its structure. By comparison H20E epoxy has a thermal conductivity between 2.5-29 W/m·K and is therefore much more effective at spreading heat.

Convection is also important and is used in the simulations in section 5.4. It defines the heat transfer from the exposed surfaces to the air surrounding the test fixture. The convection coefficient used is defined within Ansys Workbench. The convection coefficient used for the purposes of the simulations is the “Stagnant Air – Horizontal Cyl”. This option provided the most accurate results in the case of the presented data. Figure 5.1 shows the plot of the convection coefficient vs temperature.

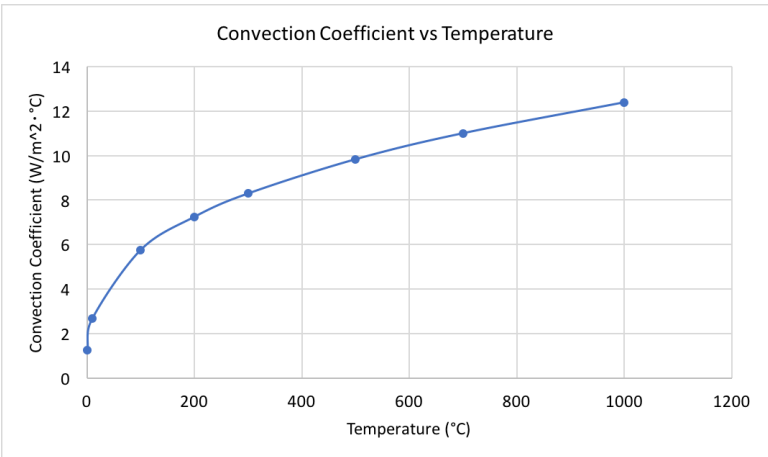


Figure 5.1 Convection coefficient vs temperature used in Ansys Workbench

Glass transition temperature is a material property that describes the point at which material begins to flow or becomes rubbery material instead of a hard and glass like material [23]. Operating at or exceeding this temperature will cause issues with adhesion between layers as well as mechanical stresses such as warping.

5.3 Thermal and RF Measurements

DDM technology is still relatively new to the microwave community and a lot of questions remain unanswered. Increasing frequency presents new challenges as does increasing power and temperature. In this section, a Ku band power amplifier's temperature and RF performance will be investigated. The device under test is the Qorvo TGA-2527SM power amplifier. A test fixture design for the PA is provided in the device data sheet [24]. The test fixture uses an 8 mil Rogers RO4003 substrate with a relative dielectric constant of 3.38. As previously mentioned, 100% in-fill ABS has a lower dielectric constant of 2.423. To maintain the characteristic impedance of the transmission lines, the substrate height was decreased to 5 mils. The resulting test board is shown in Figure 5.2.

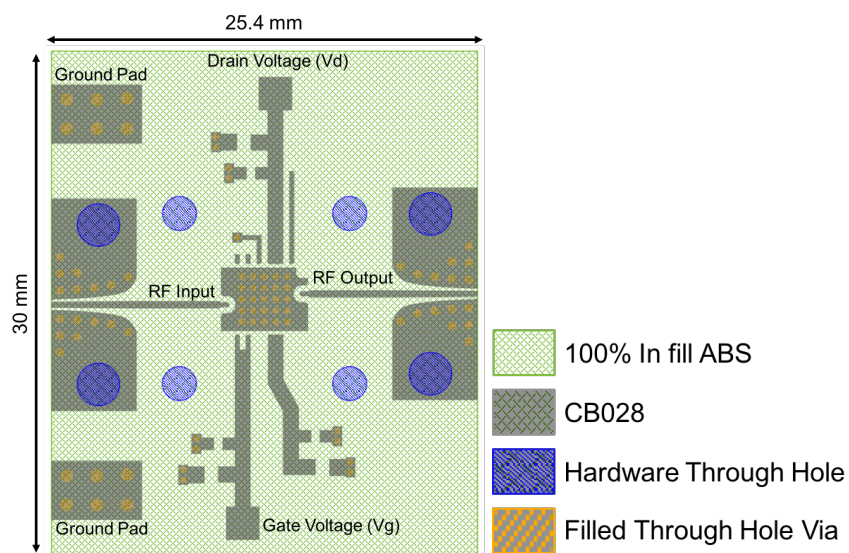


Figure 5.2 Modified test board used for an ABS substrate

A study of the RF and thermal performance is investigated through the variation of the number of vias used for the ground pad of the PA. The two configurations used have either 25 or 16 thermal vias (Figure 5.3).

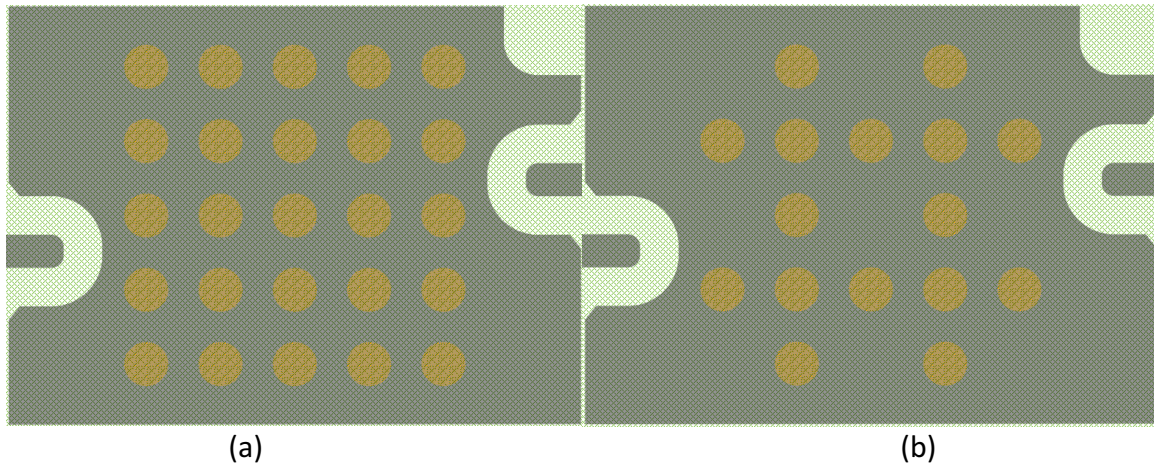


Figure 5.3 Designs with varying via numbers. (a) 25 via design (b) 16 via design

The components and values used in the bias networks are documented in the device datasheet [24]. The connectors used for the test fixture are the Southwest Microwave 292-04A-5 male SMA end launch connectors. The fabricated and assembled test board is shown in Figure 5.4. A brass carrier is used to diffuse the high temperature away from the PA. The proper bias conditions for the PA are: Drain Voltage = 6V, $I_d = 650\text{mA}$ and $V_g = -0.55\text{V}$.

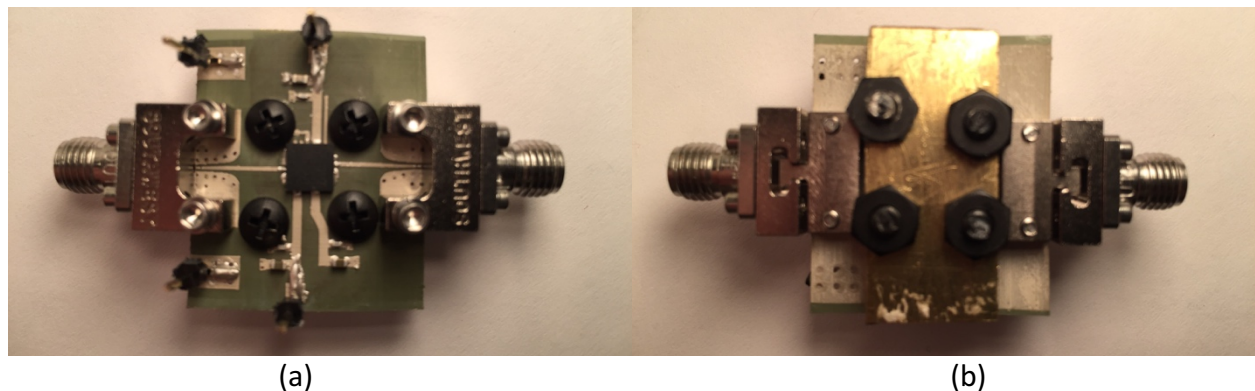


Figure 5.4 Fabricated design with a carrier and Southwest Microwave connectors attached. (a) Top view (b) Bottom view

For the thermal testing two different test are performed: 1) The PA is terminated in 50 Ohm loads and DC biased. 2) The PA is placed in the measurement system of Figure 5.5 and tested with the application of a 14GHz CW signal.

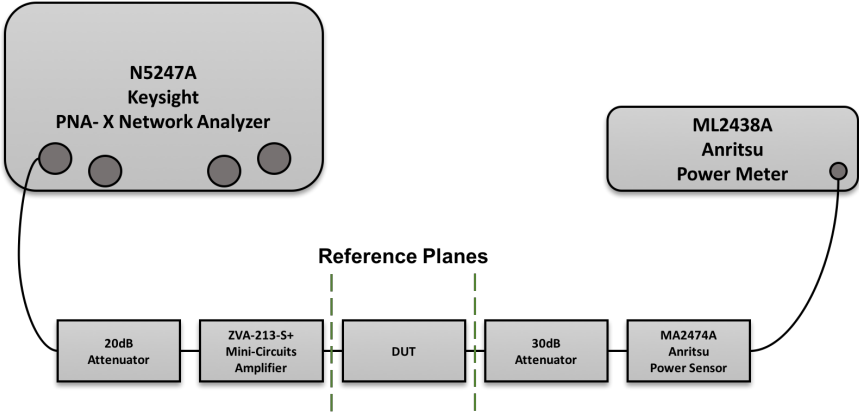


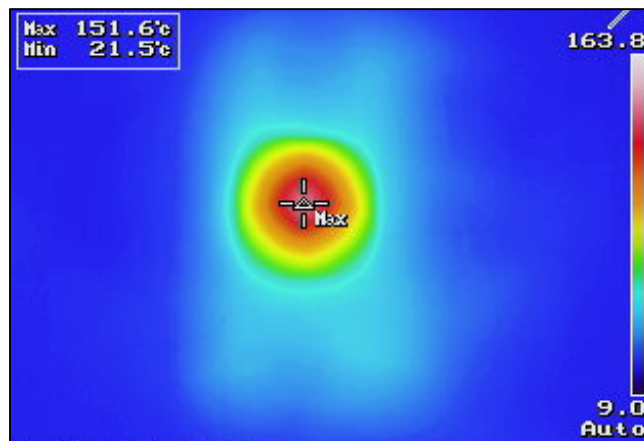
Figure 5.5 Measurement setup for the PA

For the DC thermal testing, the PA is biased at different drain currents to determine the typical temperatures for each bias condition. Since the glass transition temperature of ABS is 105°C, it’s important to determine if the substrate approaches that value. The temperature is measured from the top of the test fixture using the Keysight U5855A TrueIR Thermal Imager.

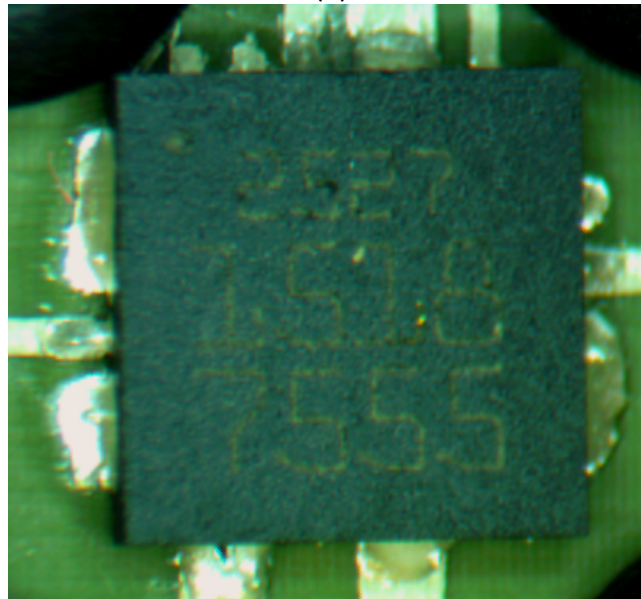
For temperature testing under DC bias conditions the device was biased and a thermal image was taken after the temperature had stabilized. Between each bias condition the PA is turned off and allowed to return to room temperature before the next bias condition is applied. Table 5.1 summarizes the DC bias results for both the 16 and 25 via designs. While testing the 16 via design it was determined that bias condition 5 results in the melting of the 100% in fill ABS substrate, at approximately 151°C. Figure 5.6 shows a thermal image of the device and an image of the damaged device.

Table 5.1 Temperature data of the two designs while operated over various bias conditions. The temperature data was collected from the top of the chip, with a thermal imager.

Bias Condition	Drain Current (Id)	Temperature (16 via hole)	Temperature (25 via hole)
1	50mA	56 °C	39 °C
2	100mA	75 °C	60 °C
3	150mA	103 °C	76 °C
4	200mA	124 °C	91 °C
5	250mA	151 °C	107 °C



(a)

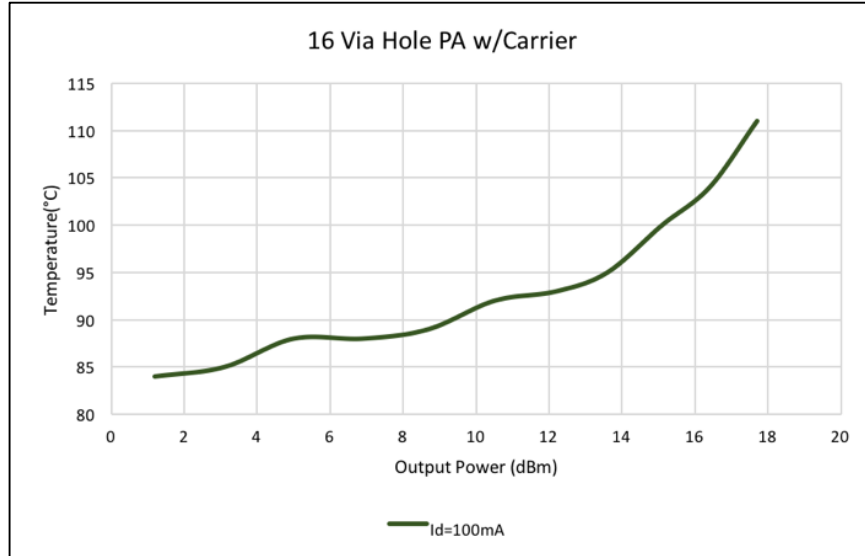


(b)

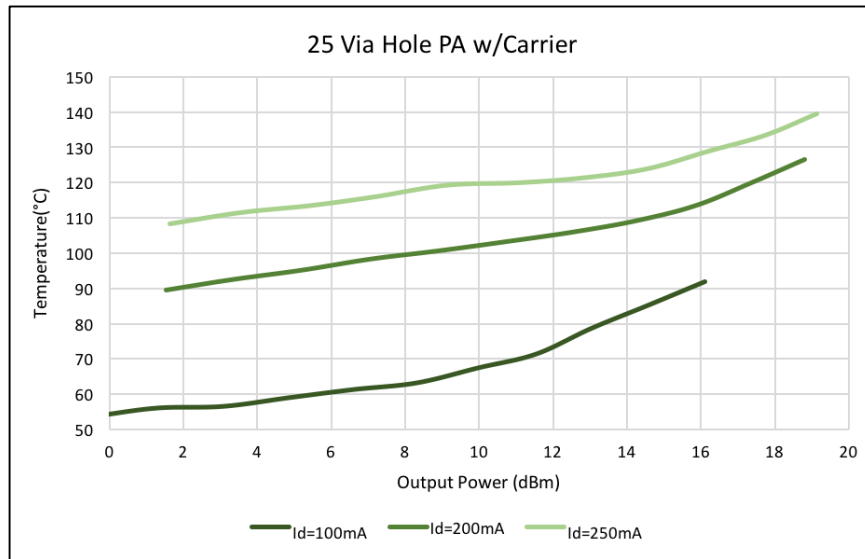
Figure 5.6 Images of the 16 via design at bias condition 5.
(a) Thermal image (b) Microscope Image

There are two possible explanations for why the substrate does not melt when the thermal temperature reaches 105°C: 1) The temperature is measured from the top, which could be measuring the channel temperature of the die vs the temperature at the ground of the device, and/or 2) The ground is melting but it is not detected due to the chip covering the ground pad and surrounding area underneath the chip. To test this, the carrier is removed and the temperature is measured from the bottom of the test fixture. Unfortunately, the heat is not diffused away from the device efficiently and as a result the substrate melted before reaching the 150mA drain current condition. A safer way to determine the temperature underneath the device is to bias the PA with the carrier attached and wait for the temperature to stabilize. Then, turn off the device and immediately measure the temperature. The results of this technique are covered later in this section.

Table 5.1 is used to determine a safe bias condition to test the device under RF drive, Table 5.1 is used to determine a safe bias condition. Bias condition 2 is used due to the high temperature of the 16 via design. Figure 5.7 shows the temperature vs output power of the two designs. The 25 via design, with a drain current of 100mA, is about 13°C cooler than the 16 via design at 16dBm of output power. Since the 25 via design has superior thermal performance, the device is biased at multiple drain currents as shown in Figure 5.7b.



(a)

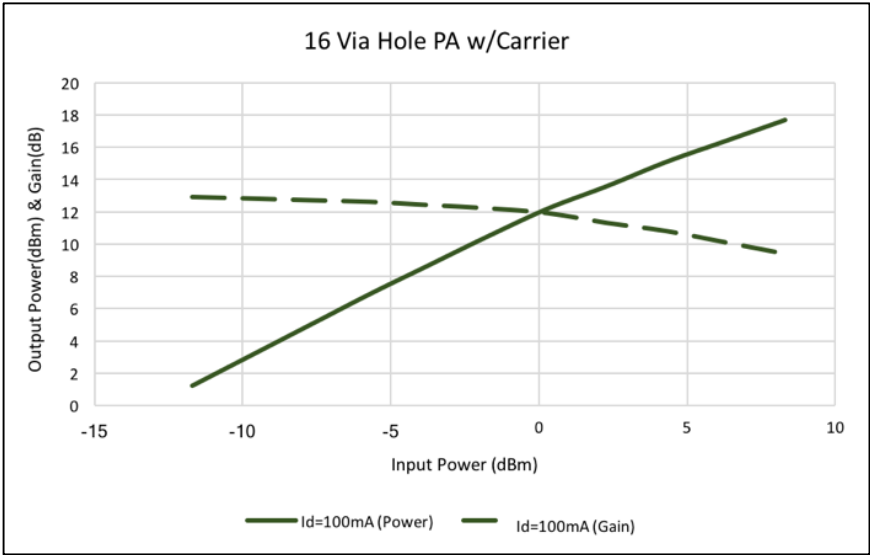


(b)

Figure 5.7 Temperature vs output power for the two designs.
 (a) 16 via design (b) 25 via hole design

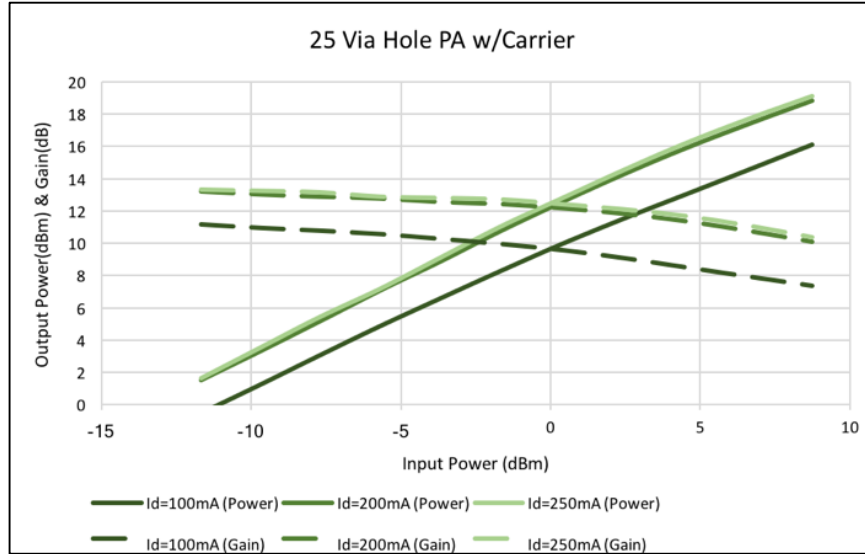
Measurements of the gain, output power and the associated temperatures under the safe operating conditions of the PA are performed. Like DC testing, the temperature is allowed to stabilize before a temperature measurement is taken. Unlike DC testing, the temperature needs to be sampled at each input power of all bias conditions. The device is returned to room temperature between bias conditions not between input power changes.

The system setup for the RF and temperature testing is shown in Figure 5.5. The VNA output power is varied from -15 dBm to 5 dBm with increments of 2 dBm. A 20 dB attenuator is added to the system to ensure the Mini-Circuits amplifier isn't driven into compression. The Anritsu power meter (ML2438A) is calibrated to ensure accurate measurement of the powers through the system. The output power of the Mini-Circuits amplifier is measured with an Anritsu power sensor (MA2474A) and Anritsu power meter. These powers are used to determine the input powers of the PA. A 30 dB attenuator is added between the PA and the power sensor to prevent any damage to the test equipment. The output power of the VNA is varied and the output power of the PA is measured. The gain and output power vs input power are calculated and are plotted in Figure 5.8 for both PA designs. The PA doesn't achieve the performance provided in the datasheet. Due to the temperature limitations, the PA can't be biased to the recommended bias conditions. A material with a higher glass transition temperature would extend the performance of the amplifier.



(a)

Figure 5.8 Output power and gain vs input power for the two designs.
 (a) 16 via design (b) 25 via hole design



(b)

Figure 5.8 (Continued)

When biasing the PA to $I_d = 250 \text{ mA}$ the device reaches a maximum temperature of approximately 140°C . To determine whether it's the die itself or the substrate that is reaching this temperature a different test is performed. The PA is powered on to a bias condition of $I_d=250 \text{ mA}$. After the temperature stabilizes a thermal image is recorded. The device is then powered off and another thermal image is recorded. If the temperature is near the temperature of the device when it is on, it can be concluded that the substrate is that temperature. However, if the temperature is substantially lower, then it can be concluded that the device is the contributor to the thermal profile and the amplifier can be driven to higher temperatures. Figure 5.9 and 5.10 show the thermal image and profile of the DUT while the device is on and directly after the device is turned off, respectively. Figure 5.9b shows a maximum temperature of 140°C when the device is on. Figure 5.10b shows a maximum temperature of approximately 73°C directly after the device is turned off. Figure 5.10a suggests that the temperature of the substrate isn't reaching the

temperature of Figure 5.9a. However, depending on the thermal transient response of the material, the temperature may change too quickly to detect with the thermal imaging method.

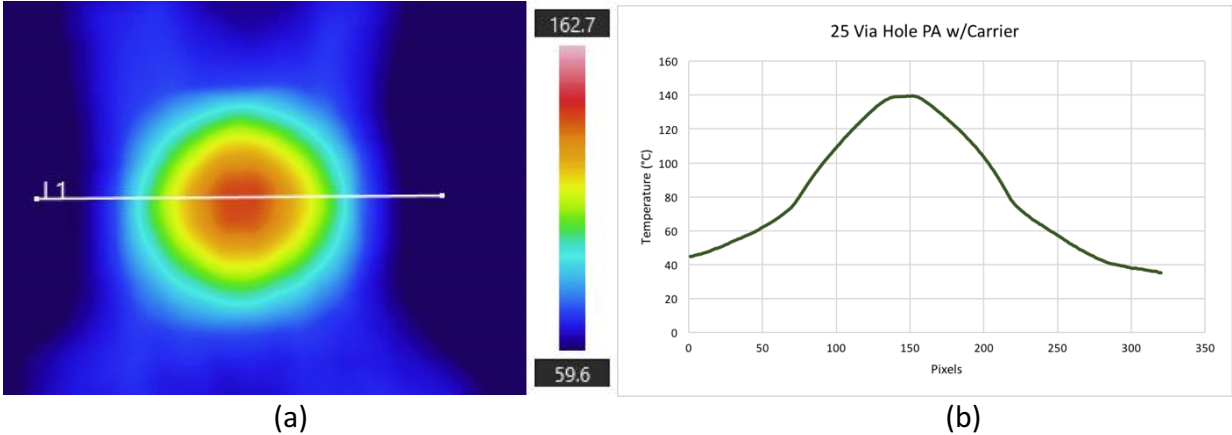


Figure 5.9 Thermal image and temperature profile with the PA on. (a) Thermal image of the PA test board with carrier at 250 mA (Id) (b) Temperature distribution along the line of the thermal image

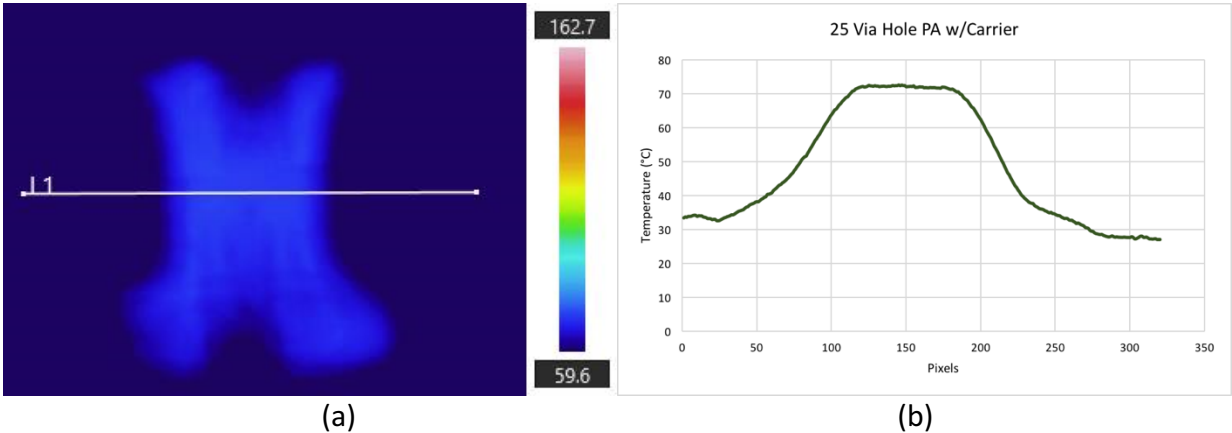


Figure 5.10 Thermal image and temperature profile with the PA off. (a) Thermal image of the PA test board with carrier, turned off after Figure 5.9 image is taken (b) Temperature distribution along the line of the thermal image

The limiting factor of the PA is the temperature at which it can operate. A few solutions to this problem are possible: use a material that has a higher glass transition temperature, design a heat sink to pull heat away from the top of the device, or possibly electroplate the epoxy elements. To determine the most effective approach, a simulation model can be used to find the most feasible option.

5.4 Power Amplifier Thermal Study

In this section, the thermal performance of an amplifier model is investigated. The ability to model and predict the performance of an amplifier is invaluable. The model is validated using measurement data. A validated model allows the designer to determine the thermal behavior of the amplifier with changes in the number of vias, the substrate materials, and the use of a carrier/heat sink. It is shown that all the above design variables can be modeled with software to perform tradeoff analysis of a given design.

The topology of a generic quad flat no-leads (QFN) package is shown in Figure 5.11. In this topology, a MMIC die is epoxied to the package grounding pad with wire bonds connecting the various parts of the chip to the package pads. The entire die including wire bonds is encapsulated in the package case. This QFN amplifier topology is mounted to a printed circuit board (PCB) using solder or epoxy. The PCB has a large ground plane and thermal vias to diffuse the heat generated on the die away from the chip. Lastly, a carrier/heat sink is used to increase the flow of heat away from the package.

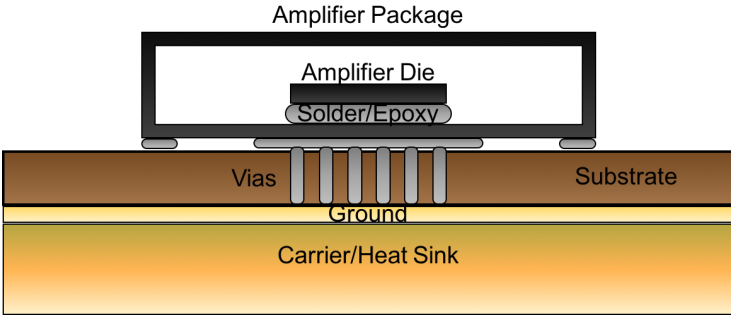


Figure 5.11 Basic topology of the QFN package mounted on a substrate and carrier

The 1 W Ku-band PA is modeled along with a 5 mil DDM PCB and brass carrier in Ansys Workbench (Figure 5.12). The various materials, thermal conductivities and glass transition temperatures are listed in Table 5.2. Additionally, various PA structures and dimensions are

shown in Figure 5.13. It should be noted that the dimensions of the package and the ground pad of the package are the only dimensions given in the datasheet. Therefore, some approximations were used and these approximations were tuned to match measurement data.

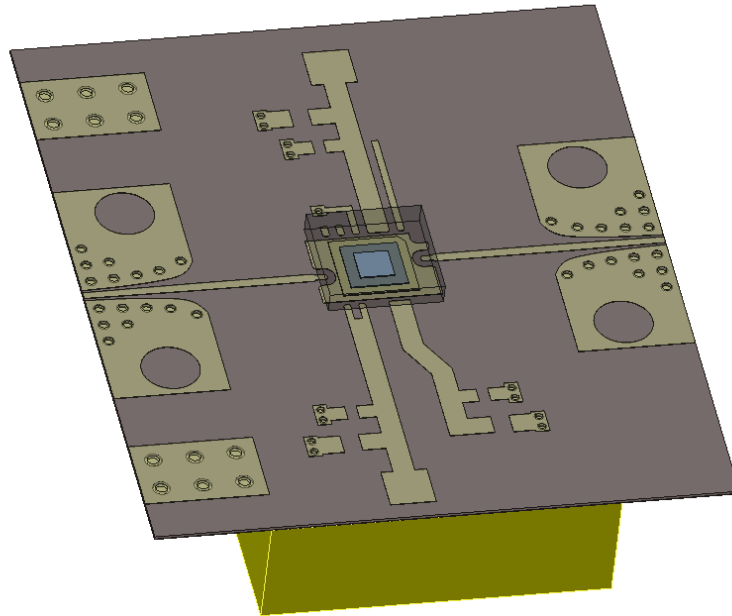


Figure 5.12 Ansys Workbench view of the simulation model

Table 5.2 Material properties of the various components of the PA test fixture

Part	Material	Thermal Conductivity (W/m·K)	Glass Transition Temperature (°C)
Package	Polyethylene	0.4	-
Die	GaN	260	-
Epoxy	H20E	2.5	>80
Vias	H20E	2.5	>80
Ground Package	Tin	64	-
Substrate	100% In-fill ABS	0.22	105
Substrate	Stratasys ULTEM 9085	≈0.22	186
Substrate	Stratasys ULTEM 1010	≈0.22	215

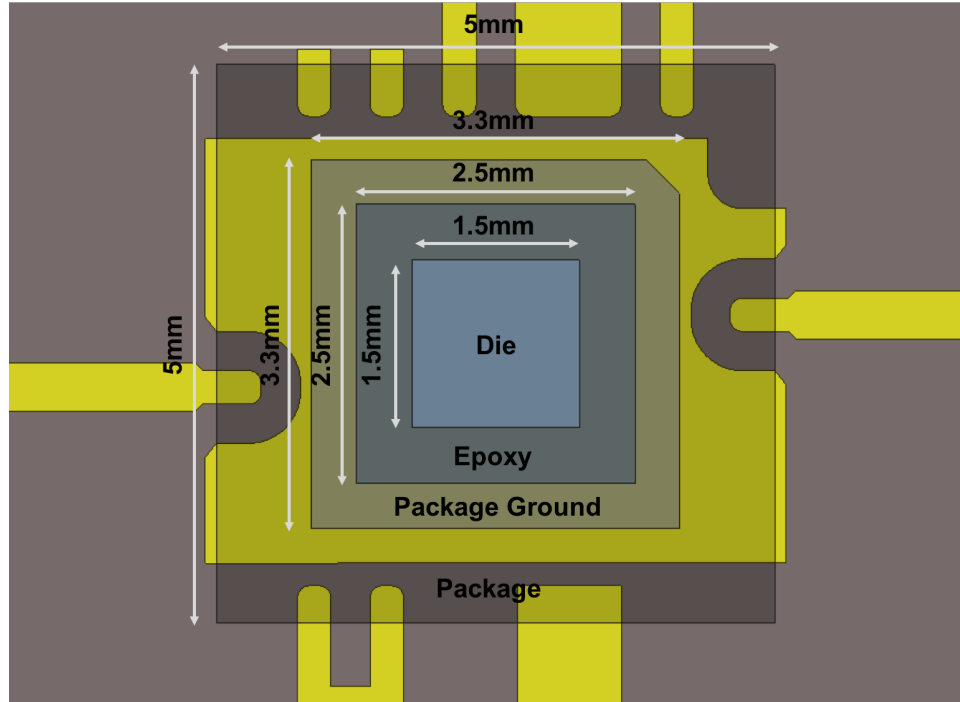


Figure 5.13 QFN stack up and the associated dimensions

Various boundary conditions are used to model the PA test fixture. A 1.5W thermal source is applied to the top face of the die. The source power is determined by the drain current and voltage. All other exposed surfaces are assigned a convection boundary. Each touching component is assigned a “bonded” interface. This boundary does not assume any thermal resistance. All heat will travel across component interfaces unperturbed, in the normal direction. The simulation results of the 25 and 16 via design are shown in Figure 5.14 and 5.15, respectively. The results are compared to the physical results for bias condition 5 in Table 5.1. The maximum temperature of the 25 via hole model is close to the physical model. However, the 16 via design varies by 32°C from simulation to measurement. A few causes that can explain this variation are discussed next.

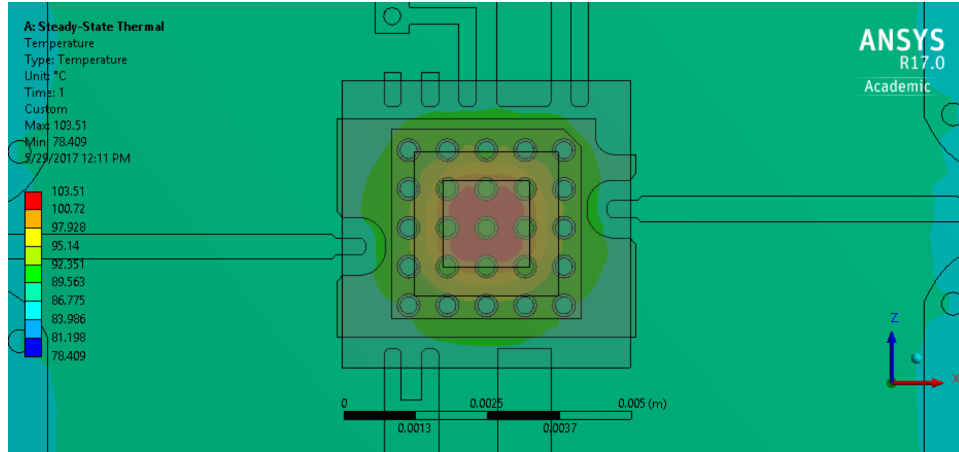


Figure 5.14 25 via hole design with a 1.5W heat source applied to the top face of the die.
Temperature range: 78.409°C – 103.51°C

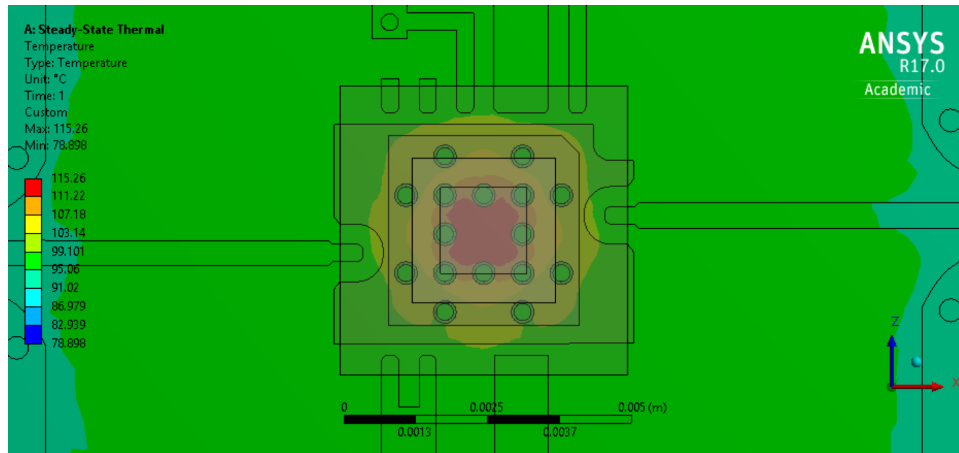


Figure 5.15 16 via hole design with a 1.5W heat source applied to the top face of the die.
Temperature range: 78.898°C – 115.26°C

The differences between the 16 via design measurement and modeled performance can be explained by studying the effects of epoxy area and conductivity. When assembling QFN packages, the amount of epoxy used and whether the chip was pressed flat will determine the footprint of the epoxy (Figure 5.16). The curing temperature and time used for the epoxy will affect the conductivity of the epoxy. As a result, the thermal diffusion away from the chip will be reduced, increasing the overall temperature. Two simulations will be performed to demonstrate the effects that the epoxy area coverage and conductivity have on the thermal properties of the

PA.

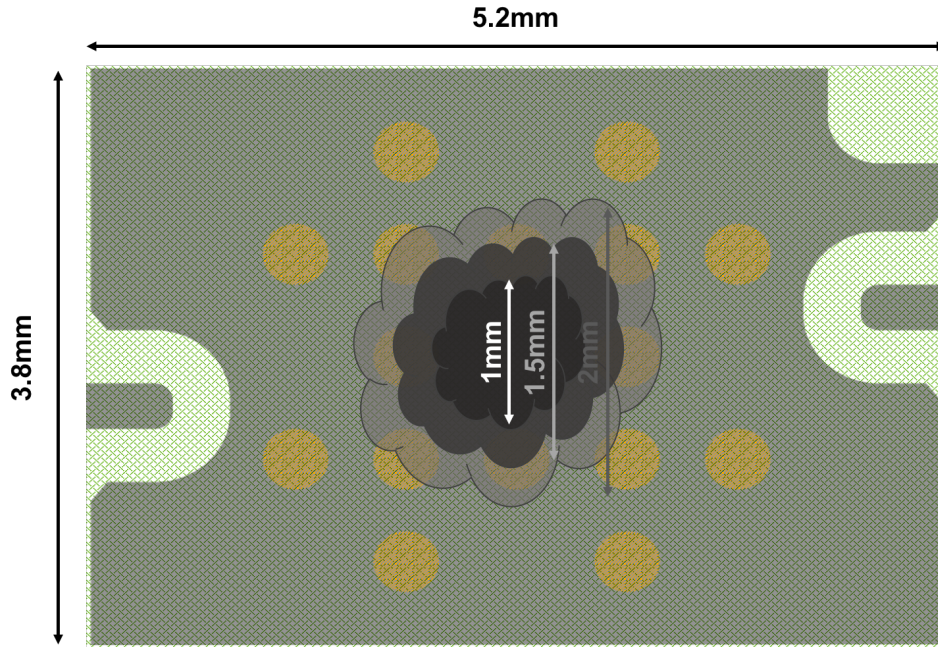


Figure 5.16 PA pad layout with varying epoxy areas

An epoxy interface is added between the PA ground pad and the PCB thermal pad. The width and height of the epoxy interface will be varied to show the temperature changes caused by each configuration. The lengths and widths are equal varying from 1 mm to 2 mm at 0.5 mm steps. Figures 5.17 - 5.19 show the simulation results of the 16 via design with 4 mm^2 , 2.25 mm^2 and 1 mm^2 areas, respectively. As the size decreases the maximum temperature increases. While the temperature does increase the maximum temperature, the temperature at the edges of the PA footprint isn't large enough to result in the ABS melting as experienced experimentally. The area does still contribute to the temperature increase. However, the area alone cannot be the cause of the temperature difference between the model and measurement data.

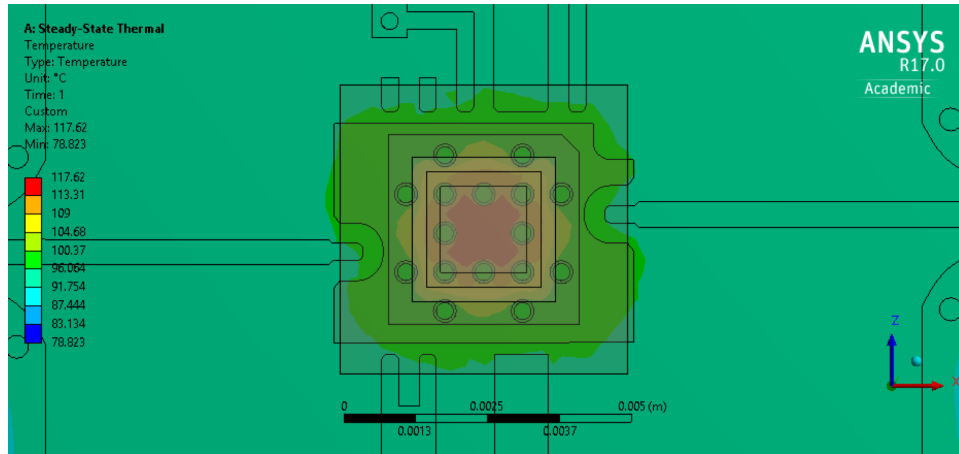


Figure 5.17 16 via hole design with 1.5 W applied to the top face of the die and a 4 mm² epoxy area. Temperature range: 78.823°C – 117.62°C

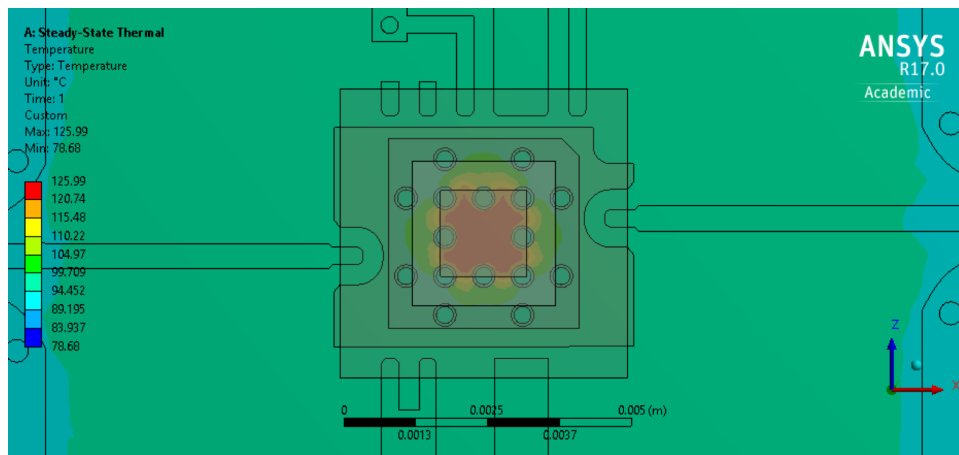


Figure 5.18 16 via hole design with 1.5 W applied to the top face of the die and a 2.25 mm² epoxy area. Temperature range: 78.68°C – 125.99°C

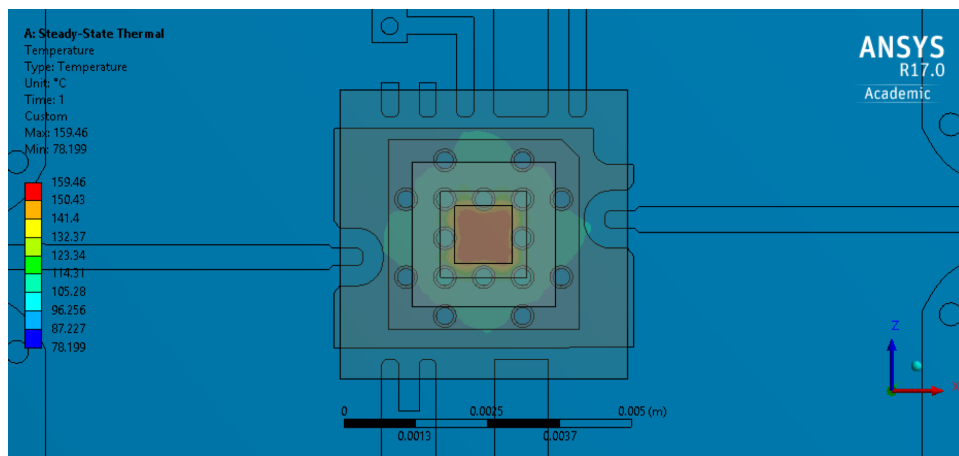


Figure 5.19 16 via hole design with 1.5 W applied to the top face of the die and a 1 mm² epoxy area. Temperature range: 78.199°C – 159.46°C

Another cause of the model vs measurement differences is the changes in the epoxy conductivity. Depending on the cure temperature, time, and number of cycles the conductivity of the epoxy can change. According to Epotek H20E datasheet, there are two different thermal conductivities, 2.5 W/mK and 29 W/mK [6]. The lower value is measured using the Laser Flash method. Where the larger value is based on thermal resistance data [6]. Three values are chosen between this range to determine the effect of conductivity on the thermal performance and what conductivity may contribute to differences of the model to measurement. Figures 5.20-5.22 show the simulation results of the PA with conductivities of 29, 15, and 5 W/mK, respectively. The simulations show that this may be a more plausible explanation for the measurement differences. Although, it may be a combination of both the area of the applied epoxy and the conductivity due to curing configurations. Based on this analysis, the thermal conductivity used for H20E is 29 W/mK and the epoxy area is 10.9 mm² (area of QFN ground pad).

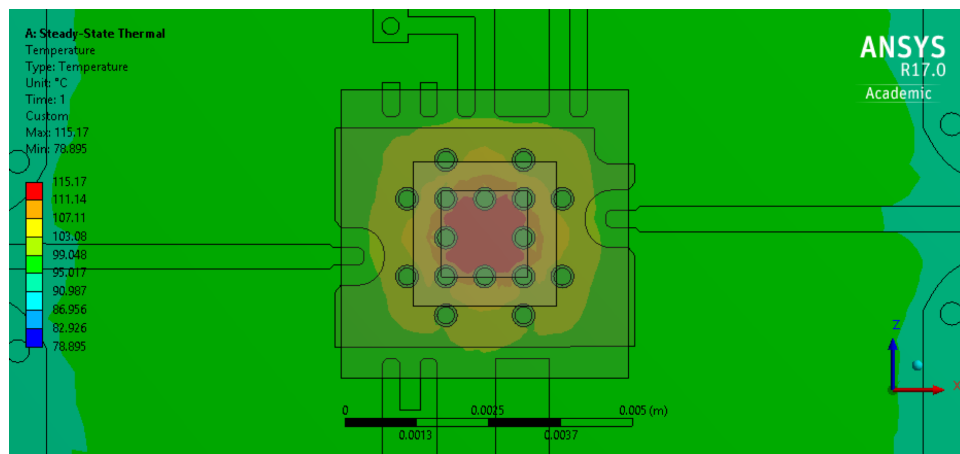


Figure 5.20 16 via hole design with 1.5 W applied to the top face of the die and a thermal conductivity of 29 W/mK. Temperature range: 78.895°C – 115.17°C

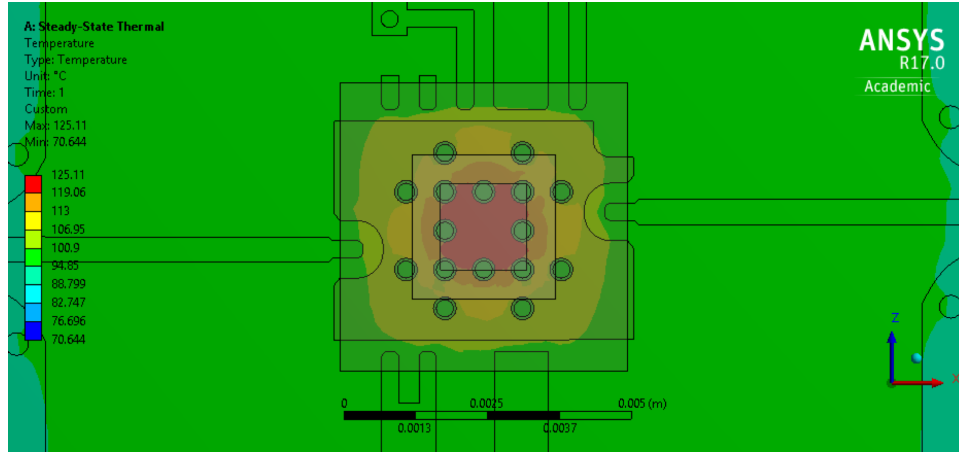


Figure 5.21 16 via hole design with 1.5 W applied to the top face of the die and a thermal conductivity of 15 W/mK. Temperature range: 70.644°C – 125.11°C

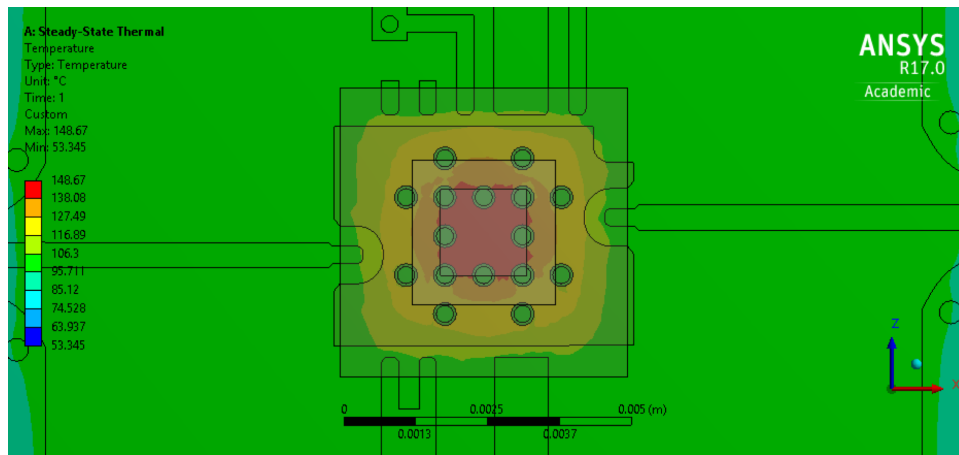


Figure 5.22 16 via hole design with 1.5 W applied to the top face of the die and a thermal conductivity of 5 W/mK. Temperature range: 53.345°C – 148.67°C

To demonstrate the 25 via model accuracy, Figure 5.23 shows the modeled vs measured thermal performance over multiple power dissipation ranges. The plot shows that over the bias conditions of Table 5.1, the model predicts the performance. The data validates the thermal model and provides certainty in the accuracy of the 16 via model, although the data does not match exactly.

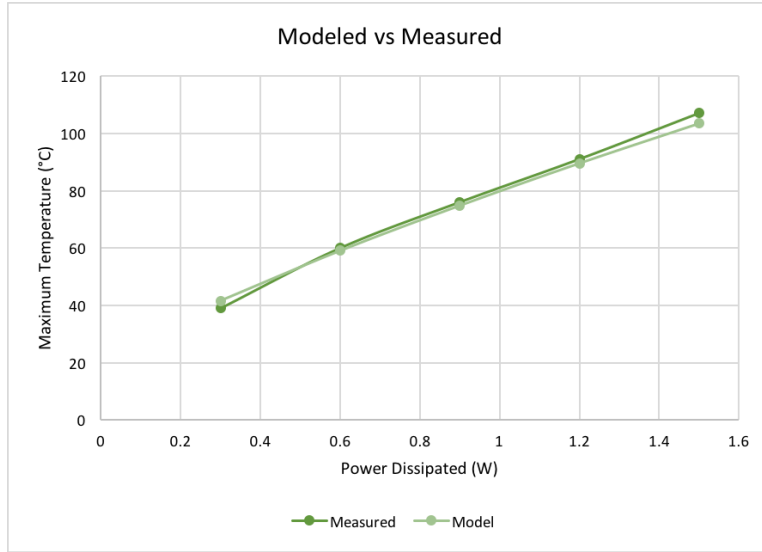


Figure 5.23 Maximum temperature vs power dissipated for the 25 via design

With the model verified, it can be used to determine a substrate suitable for high temperature operation. The power dissipation is increased to 3.5 W to simulate the PA working at the proper bias condition and under RF drive. Figures 5.24 and 5.25 show the simulation results of the 25 and 16 via designs, respectively. Table 5.2 shows the material properties of two different types of ULTEM materials. Both materials can be used in the future for the PA assuming the design uses 25 vias and a carrier. Figure 5.26 shows the simulation results of the 25 via design, with 1.5 W of power dissipation without a carrier. Figure 5.26, shows that a carrier needs to be used, whether it's metal or another material with a high thermal conductivity.

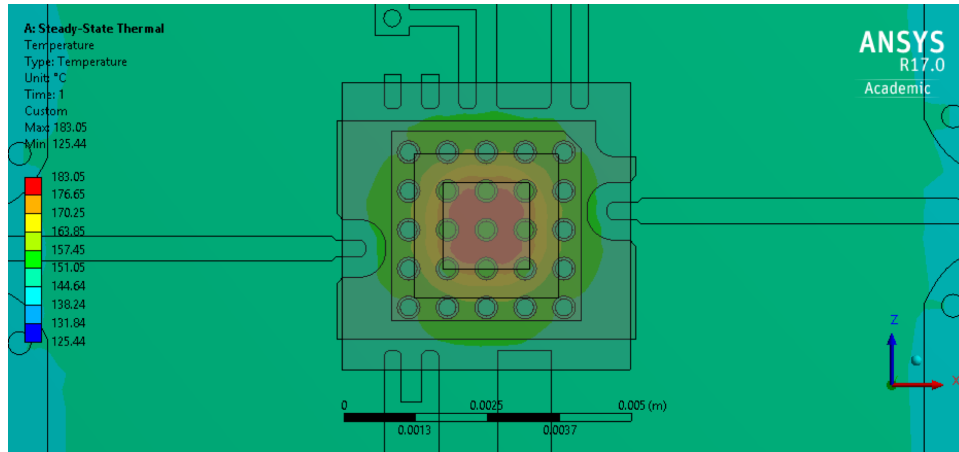


Figure 5.24 25 via design with 3.5 W applied to the top face of the die.
Temperature range: 125.44°C – 183.05°C

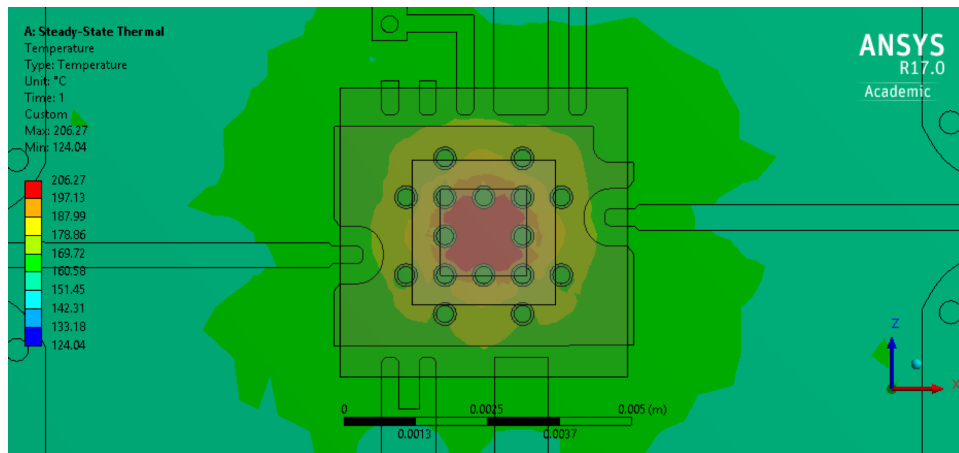


Figure 5.25 16 via design with 3.5 W applied to the top face of the die.
Temperature range: 124.04°C – 206.27°C

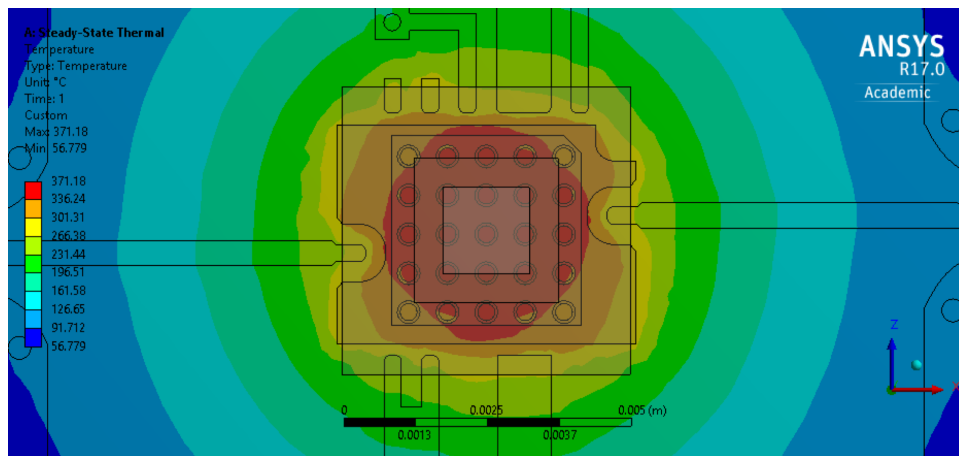


Figure 5.26 25 via design with 1.5 W applied to the top face of the die without a carrier.
Temperature range: 56.779°C – 371.18°C

5.5 Conclusion

As the trend of higher power and smaller devices grows DDM technology needs to adapt to accommodate these changes. The limiting factor of power amplifiers on DDM PCBs is the temperature that the thermoplastic can handle. The RF performance suffered due to the temperature limitation. However, it's possible that if a different thermoplastic is used that the PA would be able to be biased at its proper voltage and current level. The model created in Ansys Workbench allows the designer to determine whether a specific substrate or carrier/heatsink configuration will improve the thermal performance.

CHAPTER 6: CONCLUSION

6.1 Summary

In summary, DDM technology shows promise in the RF and microwaves field. The ability to create highly customized low cost RF circuits is invaluable. Chapter 3 shows that the overall size of the DDM hybrid coupler is slightly larger than traditional PCB coupler. However, if a thermoplastic with a higher relative dielectric constant is used the size difference wouldn't be as substantial. The performance between the PCB and DDM couplers were similar, showing promise for 3D printed RF components at 2.45 GHz.

Chapter 4 covered the design, measurement and modeling of the DDM Ku band connector. The ability to tune the connector using the TDR tool is invaluable. It provides insight into what is happening within the connector at discontinuities. The DDM connector has less than 0.45 dB of insertion loss up to 14 GHz and less than 10 dB of return loss up to 15 GHz. Even though the connector showed issues with the transition, the performance is still reasonable for a first iteration design.

Chapter 5 demonstrated the thermal performance of the PA test fixture with a varying number of vias. A thermal model was created in Ansys Workbench which demonstrates agreement between simulated and measurement data. The ability to use this model to switch material types is invaluable in the evaluation of future tests. Work still needs to be done in the

high-power amplifier field of 3D printing. But, the work of Chapter 5 provides a foundation for future research.

6.2 Recommendations for Future Works

Follow on work in the areas of Chapters 4 and 5 will be beneficial to the future of DDM. A major issue that arose in the connector manufacturing is the printing of the embedded transition in Chapter 4. Spraying conductive ink would solve a lot of the issues with the transition. A different connector or orientation would also be good suggestions. A SMP or SMP-M would probably be a good alternative. SMP-M has an upper operating frequency of 40 GHz which would push 3D printing to higher frequencies. Finally, end-launch designs should be considered for future work.

Chapter 5 future work would include further development of a thermal model for the PA device. Validating the model to measurement data for multiple thermoplastics. The model could be further developed by a mechanical engineer to provide a modeling process for chips of different powers and material technologies.

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APPENDIX A: SIMULATION AND ASSEMBLY

A.1 Introduction

Throughout the research there was multiple lessons learned when pertaining to simulations and assembly of DDM parts. From meshing options to the do's and do not's of assembling with epoxy. Section A.2 will cover the simulation issue that was experienced in the research. Section A.3 covers assembly issues and techniques used throughout the work. This appendix is written to minimize the issues that future students may run into during their research in DDM and RF design.

A.2 Simulation Issues

The major issue that was experienced with simulations was with ADS Momentum settings. A few settings can be adjusted to ensure that students do not make mistakes when trying to match simulation and measurement data. The first option (Figure A.1) within the EMSetup of ADS is the "Simplify the layout" option. This option will result in the layouts mesh being reduced. However, in doing so, the mesh will not accurately represent the circuit (Figure A.2). The cells per wavelength is set to 60 and the meshing frequency is 3 GHz. These settings are more than sufficient to solve the coupler circuit. However, since the "Simplify the layout" option is selected it overrides the cells per wavelength erroneously. The same circuit and options are used and the mesh regenerated without the "Simplify the layout" option and it is seen that the mesh is accurately following the geometry (Figure A.3). This may seem like common sense,

however when using the EM Co-simulation option the mesh isn't shown. To avoid issues, it's best to generate the mesh prior to running any simulations to ensure an accurate mesh is used.

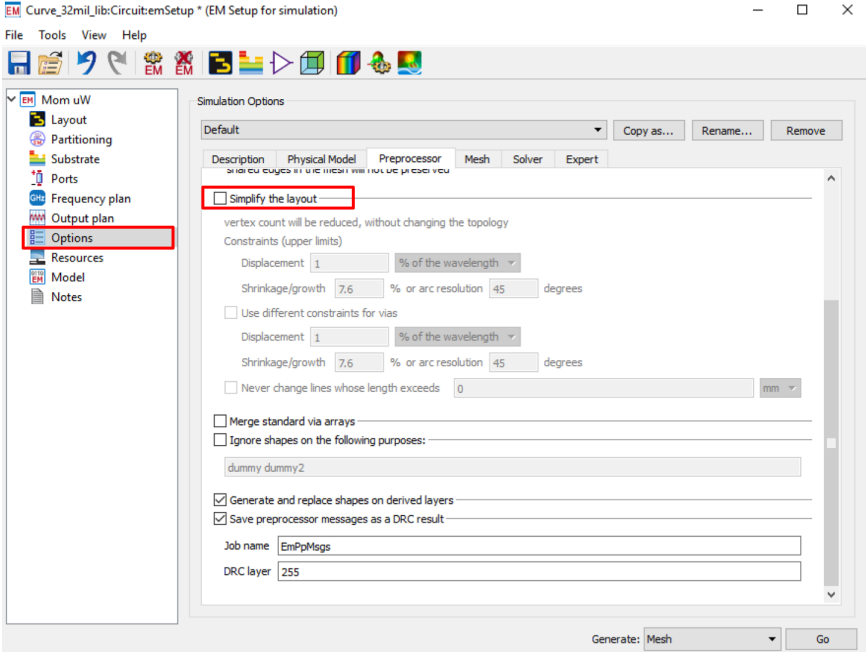


Figure A.1 EM setup options to avoid simplifying the layout mesh



Figure A.2 Mesh resulting from the "Simplify the layout" option

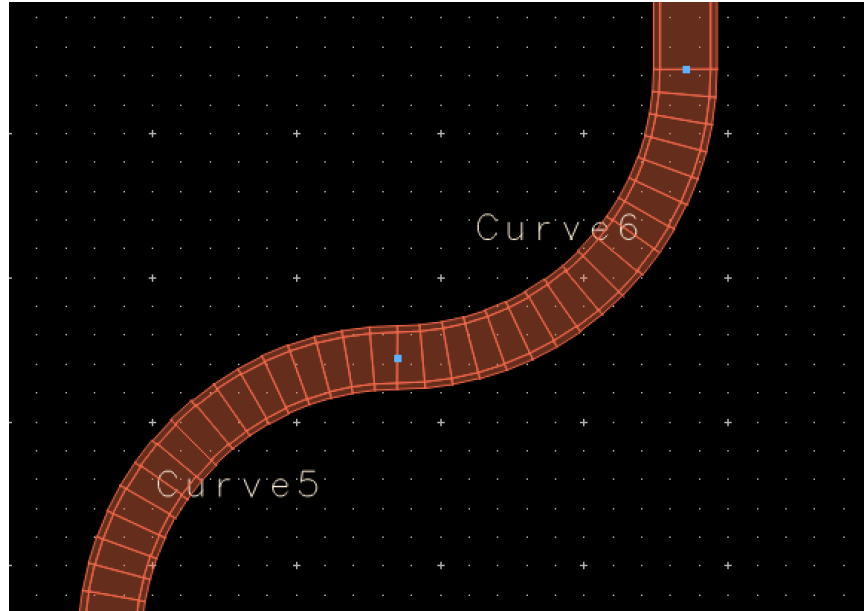


Figure A.3 Mesh resulting from not selecting the “Simplify the layout” option

The other options didn't cause errors, they are just recommendations. The cells per wavelength is obviously important because if it's too low the same result will occur as did in Figure A.2. Another setting is the edge mesh option. This provides mesh spacing between the edges and the inner conductor. It seems to provide a more uniform mesh. The final option, which is unchecked, is the “Mesh reduction” option. Although, it didn't result in an error in my circuit use this option with caution. Figure A.4 shows the effect of using the Mesh reduction.

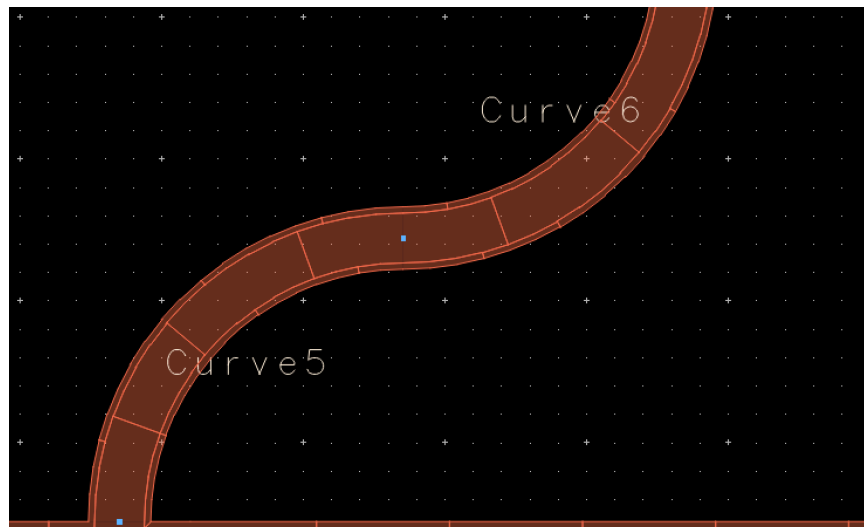


Figure A.4 Mesh resulting from selecting the “Mesh reduction” option

A.3 Assembly and Fabrication Techniques

Following a few techniques in assembly can improve the end-product of your design. The first tip is used when using a milling machine to fabricate a design. Instead of the milling machine removing the excess conductor from a laminate, it is nicer to just route the traces of the microstrip lines and use an Exacto knife to peel the excess conductor off. This isn't a technique I came up with, this is something taught to me by Yaniel Vega. This technique will improve the overall uniformity of the substrate and minimize any rough surfaces around the microstrip lines.

Assembly with H20E sometimes is quite a challenge. Having assembled over 1000 parts myself, I know how tedious the task can be. When mixing the different parts of the epoxy it is extremely important that the epoxy is mixed well. If it is not mixed properly, connectors especially, will easily separate from the substrate and transmission lines. Another consequence of not mixing properly is that the H20E seems to crack a lot easier. This cracking will cause connectors to become intermitted and ultimately cause issues with measurement data. Cure time and the number of cycles in and out of the oven is also important. With the glass transition temperature of ABS being 105°C, the temperature used to cure H20E was 87°C. Technically ABS is OK at 90°C, but as Figure A.5 shows, the adhesion between layers is often compromised. Try to reduce the number of cure cycles for the part, however this is sometimes unavoidable. If a mistake is made when mounting a lumped component or connector (e.g. shorting a transmission line gap), put the part in the oven for 1hr at 87°C or finish the other components and cure for the full duration. Remove the mistake AFTER the part has been cured. This will save a lot of time and trouble. It is a lot easier to remove the hardened epoxy than to try to remove the uncured epoxy with chemicals or by wiping it away.

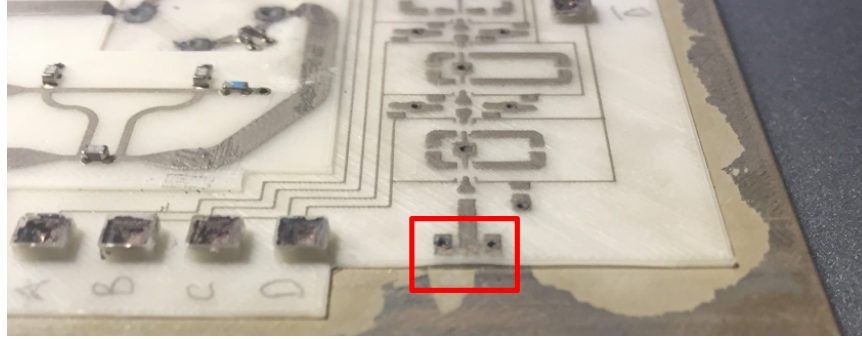


Figure A.5 Top ABS layer separating from the ground plane

When assembling QFN packages two techniques should be considered. First, fill the via holes with H2O2 prior to mounting the QFN. This will ensure all vias are connected to ground providing a thermal path for heat dissipation. Cure the vias before attaching the QFN package. If the vias aren't cured without the QFN attached the H2O2 may not fully cure reducing the conductivity. Curing the vias separately also ensures that the epoxy applied to the ground pad will be used for the attachment of the QFN device not filling the vias, possibly causing a substandard connection. Second, attach the QFN package and cure the epoxy again. If this step isn't performed, it will be extremely hard to make the pad connections without moving the package around. Ensure that the epoxy is spread in a somewhat thin layer. The epoxy spreading needs to be limited when pressing the QFN into place, to avoid shorting the ground pad and signal lines. Ensure that the QFN package is sitting as flat as possible. It isn't acceptable to have it sitting off high off the substrate. This will decrease the thermal diffusion away from the chip and likely worsen the RF performance. Lastly, make the connections to the pads. Again, it is OK if two pads short together. Just bake the circuit and remove the short after the epoxy is cured. Another advantage of assembling the QFN in multiple steps is that shorts between the ground pad and signal traces can be checked prior to connecting the pads of the package to their respective traces.

APPENDIX B: DDM CONNECTOR PRINTING

B.1 3D Printing Procedure

A single 0.1 μm base layer consisting of 100% in-fill ABS layer is printed with the first layer being 50 μm and two subsequent layers being 25 μm each. The second layer consists of a 25 μm CB028 microstrip line is micro-dispensed and dried. A mixture of ABS and acetone is used to cover the base layer and microstrip line. This mixture is used to improve the adhesion between layers containing micro-dispensed conductors and the next ABS layer. The 125 μm substrate layer is printed next (100% in-fill ABS) followed by the ground plane, which is micro-dispensed and allowed to dry. The two DDM connectors (50% in-fill ABS) are outlined using 100% in-fill ABS. The semi-circular transition is printed in a staircase fashion with a z-axis resolution of 25 μm . The CB028 paste is micro-dispense over the transition and dried. When the transition (100% in-fill ABS) is finished, the 50% in-fill layers are continued in 50 μm steps to finish the remainder of the connector. The conductive ink on the outer portions of the connectors and via holes are post processed by-hand. The mechanical structures are printed separately from the connector structure and attached using adhesive for mechanical strength. The nScript 3Dn printer can print the mechanical structures in situ. The decision to print the structures separately was due to the post processing required to ensure the connectors fit was correct.